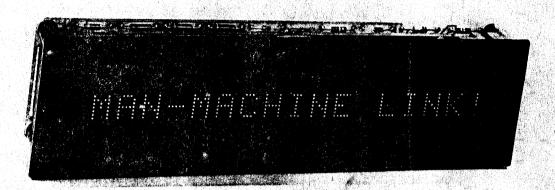
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The model SSD1000-0030 is a 16- or 18-position alphanumeric display. Each character is displayed in a 5 x 7 dot matrix with two column spaces between characters for a 16-character display, and one column space between characters for an 18-character display. The characters are displayed by presenting the appropriate 6-bit binary code to the data input lines for each character position. A repertoire of 64 different characters is contained in the character generator supplied with this display. Any given 6-bit binary input code can be cross-referenced to its associated character font in Truth Table 1. The character set in Table 1 is referred to as a 6-bit modified ASCII code. The 6-bit modified ASCII is derived from the 8-bit ASCII code by effectively eliminating the parity and lower case bits.

To display characters not found in Truth Table I, auxiliary data input lines are provided to bypass the character generator and directly access the display anodes normally addressed by the character generator.

The display operates in a scanning mode, scanning only one column of the 111 column display for each inputted clock pulse. At the start of a scan and at the end of the 111th clock period, a reset pulse must be applied to reset the display and start a new scan at column 1. The scanning of the display is done above the flicker rate of the human eye (70–80 Hz), so the display characters appear to be on all the time. Actually, only one column of dots is on at any given time.

The model SSD1000-0039 display is the same as the model SSD1000-0030 except it does not have a character generator. Instead of inputting a 6-bit binary code, the 7 auxiliary lines must be used to input dot matrix information. Using the auxiliary data input lines allows any dot matrix information presentable in 111 columns by 7 rows of dots to be displayed.

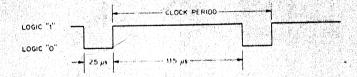
OPERATION

Reset Input — The reset input is the first input pulse applied to the display. It resets the scan section to the reset column at the extreme left-hand side of the display.

Reset occurs on the positive to negative transition of the pulse. The duration of the reset state must be one clock period to three clock periods (one clock period is recommended for optimum display life). The reset input must be applied after the 111th clock pulse in order to start a new left-to-right scan of the panel.

Data Input — These inputs are used on model SSD1000-0030 only. The six inputs are binary, positive logic, modified ASCII code. The appropriate 6-bit data input code must be present at the input terminals for the first five clock pulses of each character position. The 6-bit data input code must be refreshed for each character position every complete scan of the display.

Clock Input — The clock input is the third input to be applied to the display. The clock input period can be 125 to 150 microseconds, with 140 microseconds being the recommended pulse width. To make a complete scan of the display, 111 clock pulses are required. The clock input must be at a logic zero level for at least 20 microseconds of its period. The following illustration is the recommended clock input:



The clock can be running during reset, but the first high-tolow transition of the clock pulse must not occur less than one microsecond before or after the low-to-high transition of the reset pulse.

Auxiliary Data Inputs - These inputs are used on the SSD1000-0030 model to present characters which are not contained in the standard 64-character repertoire character generator. The model SSD1000-0039 does not have a character generator. This model requires exclusive use of the 7 auxiliary data input lines to input dot matrix information. Auxiliary data input 1 corresponds to 1st dot of 1st row.

CHARACTER FORMAT (Actual Size)

Dot matrix information is presented to the 7 auxiliary data input lines column by column. There are 111 columns contained in these displays. To display information in any specified column, clock pulses must be counted starting with the first clock pulse after reset. Each clock pulse equals one column "on" time; thus, the number of clock pulses equals the column which is being scanned. A dot can only be lit in a column which is being scanned. A logical "0" at any auxiliary data input lights a dot. The auxiliary data inputs must be held in the logic "1" state for 15 microseconds after every negative clock transition and during the entire reset period. Input data must be present for the entire "on" time of the displayed column.

Blank Disable Input — This input is used on the model SSD1000-0030 only. Information displayed may be blanked out at any time by bringing this input to a logic "1" level. This input is normally switched to ground. When using the auxiliary data inputs on the model SSD1000-0030, this input must be brought to a logic "1" level.

Update Output — Available on the model SSD 1000-0030 only. This output pulse tells you when you have reached

the end of a character position, and that it's time to apply your 6-bit data input code for the next character position. The update output has a pulse width of one clock period and goes to a logic "1" at the end of each character position.

Clock Control Input — Used on the model SSD1000-0030 only. This input determines whether the display operates in a 16- or 18-position mode. Tying this input to —12V yields an 18-character display with one column of space between characters. Tying it to +5V yields a 16-character display with two columns of space between characters.

For further information, reference this bulletin number and write to Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Plainfield, New Jersey 07061; or call one of our special sales/applications assistance numbers, (201) 757-5000 in New Jersey, or (714) 835-7335 in California. For overseas inquiries, write to Burroughs ECD International, Langwood House, High Street, Rickmansworth, Herts, England, Tel. (44) 9237-70545.

ELECTRICAL CHARACTERISTICS

Power Required Positive Logic Supply Negative Logic Supply Display Supply	4.75 to 5.25V @ 160 mA max. 11.4 to12.6V @50 mA max. +237.5 to +262.5V @ 30 mA max.
Clock Input Signal (See Figure 1) Logic 1 Level Logic 0 Level Clock Period (t ₁) Logic 0 Voltage Duration	2.0 to 5.25V @ 10 uA max. 0 to 0.8V @ -1.6 mA max. 125 to 150 us 20 us to Clock Period -20 us
Data Input Signals (SSD1000-0030 Logic 1 Level Logic 0 Level Duration	Only) 4.0 to 5.25V @ 10 uA max7.0 to 0.6V @ 10 uA max. 5 Clock Periods
Auxiliary Data Input Signals Logic 1 Level Logic 0 Level Logic 1 Duration	(Note 3) -0.5 to 0.3V @ -3 mA max. 15 us min. to 1 Clock Period max.
Reset Input Logic 1 Level Logic 0 Level Duration (t2) Reset Input Delay (t3)	2.0 to 5.25V @ 10 uA max. 0 to 0.8V @ 1.6 mA max. 1 to 2 Clock Periods 1 us
Blank Disable Input (Blanking Cor Logic 1 Level Logic 0 Level	ntrol) (SSD1000-0030 Only) 2.0 to 5.25V @ 10 uA max. 0 to 0.8V @ -1.6 mA max.
Data Update Output (Pulse Indica Logic 1 Level Logic 0 Level	ting End of Character) (-0030 Only) 4.25V min. 0.4V max.

Table 1. TRUTH TABLE (SSD1000-0030 Only)

BINARY	снав.	BINARY	СНАВ	BINARY	CHAR.
0	@	22 16	V	43 ZB	+
1	Α	23 17	W	4426	
2	В	24 18	Χ	45 2 D	-
3	С	25 19	Υ	46 ZE	
4	D	26 1 F	ŧΖ	47 2 F	
5	Ε	27 //] {	4830	Ø
6	F	28/10	\sim	. 49 31	1
7	G	29 18	} }	5032	2
8	Н	30 1€	{	51 33	
9	- 1	. 31 lF	}	523A	4
10 ₺	J	3220	BLANK	53 3	5 5
11 A	Κ	33 2	1	5430	. 6
12 C	L	34 2	٠, ،,	55 3 7	ı 7
13 0	Μ	35 73	5 #	56 3 %	8
14 E	N	36 ZA	\$	5/39	9
15 €		37 2-5	0/5	583A	
16 (0	ρ	38 26	. &	5938	;
17 / (39 %	7/	6036	(
18 / 2		40 2.8	} (6130) =
19 (3		41 25)	62 3£	-)
20 14		4221	8.	633F	?
21 15		h e e			

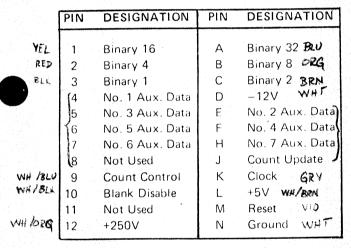
		5111	DEGLONIATION
PIN	DESIGNATION	PIN	DESIGNATION
1	Not Used	Α	Not Used
2	Not Used	В	Not Used
3	Not Used	C ·	Not Used
4	No. 1 Aux. Data	D	Not Used
5	No. 3 Aux, Data	E	No. 2 Aux. Data
6	No. 5 Aux. Data	F	No. 4 Aux. Data
7	No. 6 Aux. Data	Н	No. 7 Aux. Data
8	Not Used	(J	Not Used
9	Not Used	K	Clock
10	Not Used	L\	+5V
11	Not Used	М	Reset
12	+250V	Ν	Ground

KEYWAY LOCATED BETWEEN PINS 7 AND 8

Figure 1A. PIN CONNECTIONS, SSD1000-0039

			2.25 ± 01
			1 1
	8.50 ± 01		
A			134 MAX
/ [A B COEFHJKL MN		119

Figure 2. OUTLINE DRAWING



KEYWAY LOCATED BETWEEN PINS 7 AND 8 Figure 1B. PIN CONNECTIONS, SSD1000-0030

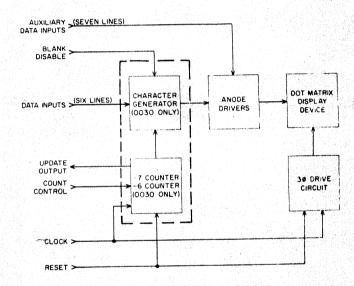


Figure 3. BLOCK DIAGRAM

ENVIRONMENTAL AND MECHANICAL CHARACTERISTICS

Operating Temperature	0° to 50°C
Storage Temperature	40° to +85°C
Relative Humidity	85% max.
(no condensation)	
Weight	10 ounces
Shock	50 g, ½ sine wave, 11 ms in
	each axis
Vibration	그리 그 그 그 그리고 그리고 말했다.
Constant	2 g acceleration, 50–2000 Hz, 30 min each axis
Sinusoid	0.018" double amplitude, 10–50 Hz
Operating Altitude	10,000 ft. max.
Storage Altitude	30,000 ft. max
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OPTICAL CHARACTERISTICS

Character Height	0.40 inch
Character Width	0.275 inch
Cell Size	0.038" × 0.0 34"
Dot Center-to-Center Spacing	0.060 inch
Luminous Intensity	100 microcandelas
Light Output	35 ft. Lamberts (Note 1)
Contrast Ratio	Note 2
Horizontal Viewing Angle	115 ⁰
Vertical Viewing Angle	70 ⁰
Color	Neon Orange

A section was in the standard process.

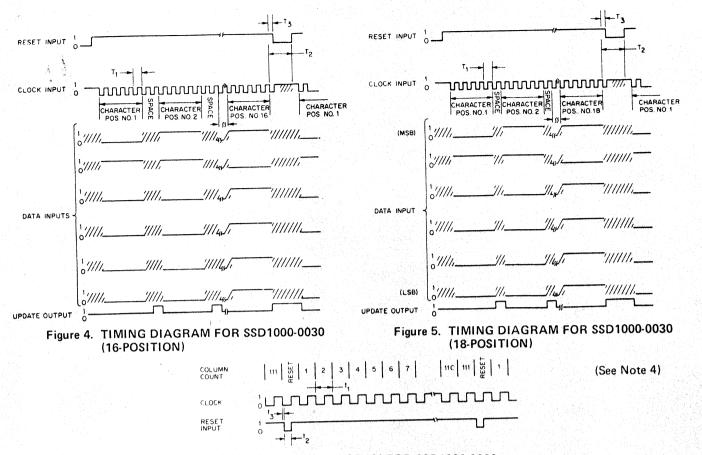


Figure 6. TIMING DIAGRAM FOR SSD1000,0039

NOTES

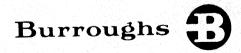
- Luminance is measured using an ICI corrected Gamma Scientific Model 2020 Photometer mounted normal to an unfiltered panel operating
 under normal drive conditions. A 0.050" diameter optical pickup is used to integrate the light from the cell cavity. The luminance
 measurement is referenced to the light output of a calibrated uniform light source masked by an aperture of the same effective glow area
 as the cell under test. (838 x 10⁻⁶ square inches.)
- 2. A suitable nonreflective matte filter is supplied with the display package which enhances the contrast ratio.
- 3. The auxiliary data input circuit configuration is the base of an NPN transistor with a grounded emitter. There are no limiting resistors between the auxiliary data inputs and the bases of the transistors; therefore, the circuits which are used to drive the auxiliary data inputs must have an impedance of no less than 2KA to 5 volts. The circuits which are used to drive the auxiliary data inputs can be an open circuit in the logic 1 state since the unit has internal pull up resistors from the base of the transistors to 5 volts.
- 4. 111 clock pulses must be generated for each scan of the display. When using 16 characters one extra column exists prior to reset. When using 18 characters four extra columns exist prior to reset.

SPECIAL INSTRUCTIONS (SSD1000-0030 Only)

Because of the MOS structure of certain circuit components, the unit is susceptible to damage from static electric discharges and voltage transients. Therefore, a shorting clip has been provided which must not be removed from the PW board until a terminated connector is wired and ready to be connected to the board. Once the shorting clip is removed the connector should be put on. Do not touch the PW wires with fingers or tools while shorting clip or connector are absent.

It is imperative that all voltages be removed from the board before removing the connector. Once the connector is removed, the shorting clip must be replaced. The connector should never be left unterminated when connected to the unit.

Recognized under the Components Program of Underwriters' Laboratories, Inc. No other reference or the Up trademark can be used.



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