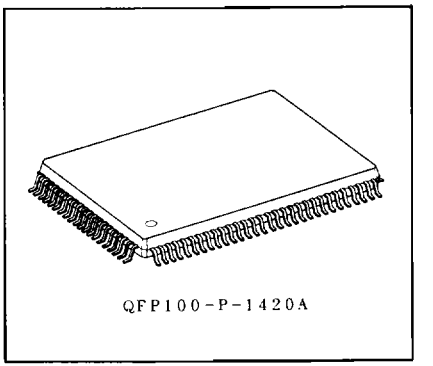
T6A34

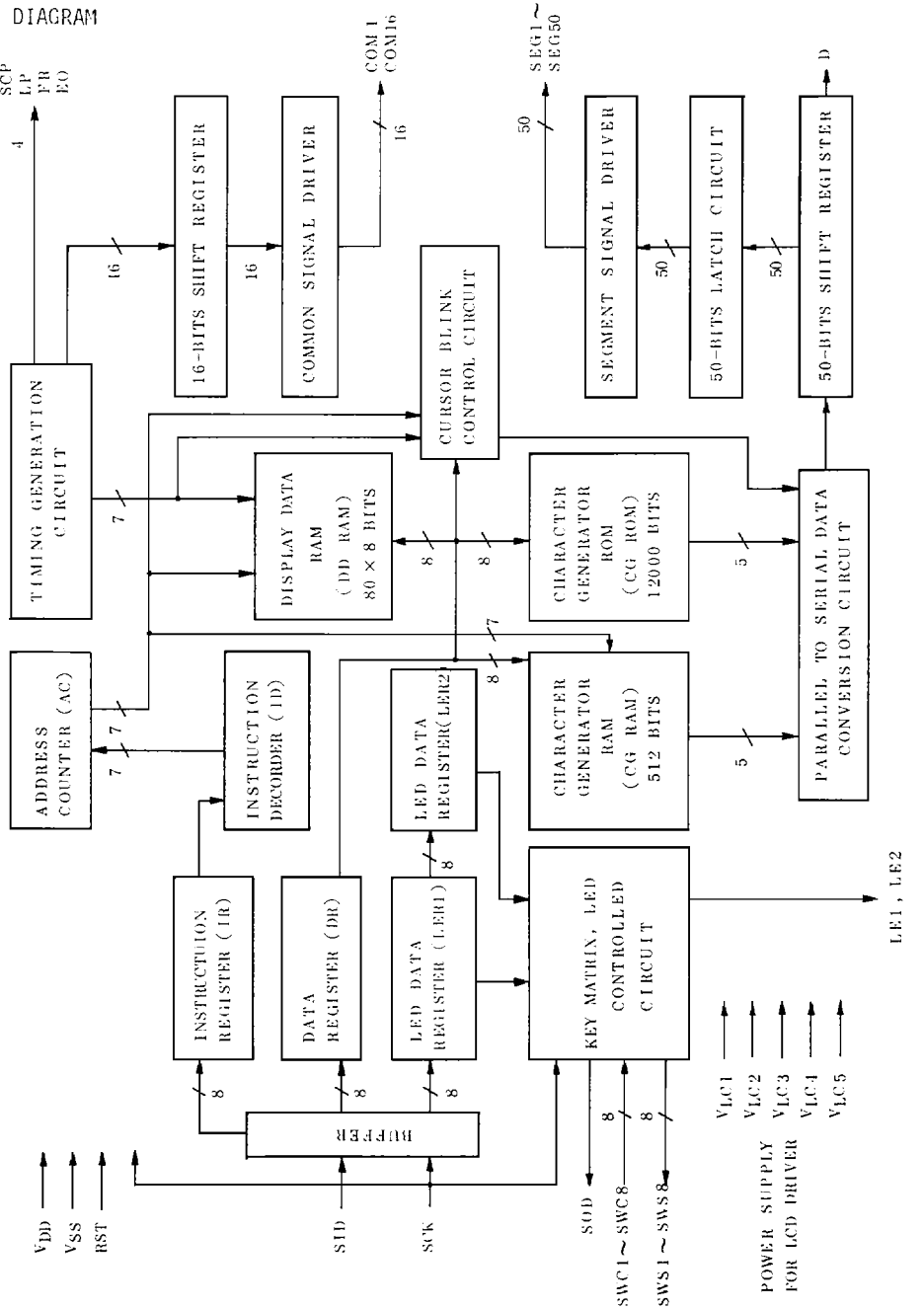
DOT MATRIX LCD CONTROLLER AND DRIVER



The T6A34 is a dot matrix LCD controller and driver.
The T6A34 is fabricated using CMOS Si-gate technology, which enables low power consumption for LCD.
Control of the T6A34 by a MPU is achieved through a serial interface, and it displays alphanumerics, kana and symbols.
The T6A34 has all the functions required for the dot matrix LCD drive. Therfore, the user can cmpose the dot matrix LCD system with less number of chips by using the T6A34.
The T6A34 is designed to be expandable with the segment driver T6A92 for conrolled 80 characters LCD.
And the T6A34 can provide a scaned interface to a 8×8 key matrix.
The T6A34 can control to a 2×8 LED matrix.

- The T6A34 can provide all signals necessaly to control the dot matrix LCD of 5×7 or 5×10 dots per one character.
- Control of the T6A34 by a MPU is achieved through a serial interface.
- Transmit clock : f_{OSC}=250kHz Typ.
- Display data RAM : 80×8 bits.
- Character generator ROM : 12000 bits.
- Charqcter generator RAM : 512 bits.
- Built in key matrix scan controller.
- The T6A34 can control to a 2×8 LED, but LED buffers is not on chip.
- Built in LCD drivers
  - 50 segments driver outputs
  - 16 commons driver outputs
- 1/8,1/11, or 1/16 duty cycle
  - 1/8 duty cycle : (5×7 dots + curor) × 1 line
  - 1/11 duty cycle : (5×10 dots + corsor) × 1 line
  - 1/16 duty cycle : (5×7 dots + cursor) × 2 lines
- Instruction functions
  - Display clear, Cursor home, Display ON·OFF, Cursor ON·OFF
  - Character blink, Character shift, Display shift Cursor shift.
- Single +5V power supply with ±10% voltage magins
- Low power consumption
- 100 pin Plastics Flat Package

BLOCK DIAGRAM



BLOCK FUNCTION

1. REGISTER

The T6A34 has four 8-bits registers. The registers are Instruction Register(IR), Data Register(DR), and two LED control data Register(LER1,LER2). The IT hold the instruction code, the address of the Display Data RAM(DDRAM), or the address of the Character Generator RAM(CGRAM). The DR hold the data to be written into the DD RAM or the CG RAM.

The data held the DR are automatically written into the DD RAM ot the CG RAM.

The LER1 and LER2 hold the controlled data of LED.

The relations between the Register Select(RS1,RS2) signals and the operation are shown in Fig. 1.

RS1	RS2	OPERATION
0	0	IR write
0	1	DR write
1	0	LER1 write
1	1	LER2 write

Fig. 1

2. ADDRESS COUNTER (AC)

The T6A34 has a 7-bits address counter. This counter assigns the address to the DD RAM, the CG RAM, and the cursor control circuit. When the Instruction code for the DD RAM or the CG RAM address set is written in the IR, the address is automatically transmited to the AC from the IR. After the data is written in the DD RAM or the CG RAM, the AC is automatically incremented or decremented.

3. DISPALY DATA RAM (DD RAM)

The display data RAM stores character codes that correspond to the character pattern. Its capacity is 80 characters × 8bits. The relation between the DD RAM address and the display position is as shown below.

The DD RAM address is expressed in hexadecimal numbers as shown in Fig. 2.

	MSB						LSB
AC	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Example: The DD RAM address=Hex 4C

MSB						LSB
1	0	0	1	1	0	0
4			C			

Fig. 2

(1) The relation between the DD RAM address and the display position in the one-line mode. (N=0)

1	2	3	4	5	.....	79	80	← The display position
00	01	02	03	04	.....	4E	4F	← The DD RAM address

a. When the T6A34 is used alome, the first 10 characters are expressed as shown below.

1	2	3	4	5	6	7	8	9	10
00	01	02	03	04	05	06	07	08	09

b. When the display shift operation is executed, the relation between the DD RAM and the display position is as shown below.

	1	2	3	4	5	6	7	8	9	10
Left shift display	01	02	03	04	05	06	07	08	09	0A

	1	2	3	4	5	6	7	8	9	10
Right shift dispaly	4F	00	01	02	03	04	05	06	07	08

(2) The relation between the DD RAM address and the display position in the 2-line display mode. (N=1)

	1	2	3	4		39	40	← Display position
1'st-line	00	01	02	03	.....	26	27	
2'nd-line	40	41	42	43	.....	66	67	← DD RAM address

Note: The last address of the 1'st-line is not continuous to the head address of the 2'nd-line.

a. When the T6A34 is used alone, the first 20 characters (10 characters×2 lines) are displayed as hsown below.

	1	2	3	4	5	6	7	8	9	10
1'st-line	00	01	02	03	04	05	06	07	08	09
2'nd-line	40	41	42	43	44	45	46	47	48	49

b. When the display shift operation is executed, the relation between the display position and the DD RAM address is as shown below.

	1	2	3	4	5	6	7	8	9	10
Left shift display	01	02	03	04	05	06	07	08	09	0A
	41	42	43	44	45	46	47	48	49	4A

	1	2	3	4	5	6	7	8	9	10
Right shift display	27	00	01	02	03	04	05	06	07	08
	67	40	41	42	43	44	45	46	47	48

4. CHARACTER GENERATOR ROM (CG ROM)

The character generator ROM is used to generate the character patterns (5×10 dots × 240 characters) from the 8-bits character codes. The relation between character codes and character patterns is shown as next page.

THE RELATION BETWEEN CHARACTER CODES AND CHARACTER PATTERN

Higher 4 bit / Lower 4 bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (0)															
XXXX0001	(1)															
XXXX0010	(2)															
XXXX0011	(3)															
XXXX0100	(4)															
XXXX0101	(5)															
XXXX0110	(6)															
XXXX0111	(7)															
XXXX1000	(0)															
XXXX1001	(1)															
XXXX1010	(2)															
XXXX1011	(3)															
XXXX1100	(4)															
XXXX1101	(5)															
XXXX1110	(6)															
XXXX1111	(7)															

5. CHARACTER GENERATOR RAM (CG RAM)

The character generator RAM is used to display user's original character patterns. (5 × 7 dots × 8 types or 5 × 10 dots × 4 types).

The relation between the character codes and the CG RAM address and character patterns is shown in Fig.3, Fig.4.

a. In the case of 5 × 7 dots character patterns

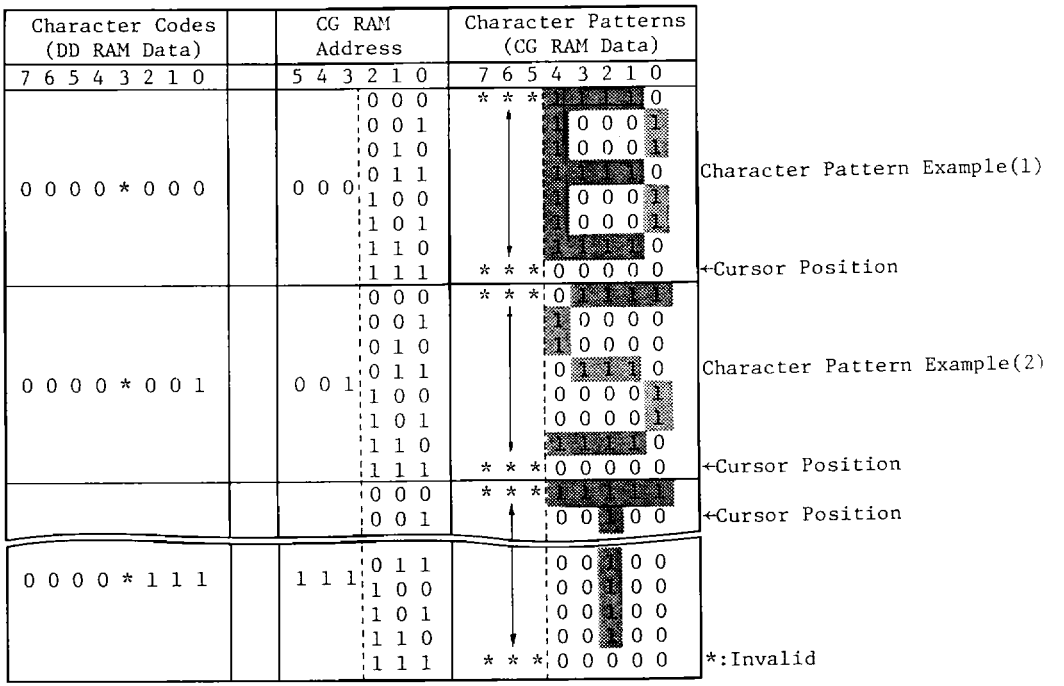


Fig. 3

Note 1: The character code bits 0-2 correspond to the CG RAM address bits 3-5.

2: The CG RAM address bits 0-2 designate the character pattern line position, The 8'th line is in the cursor position and it is displayed in logical OR by the cursor. Therefore the 8'th line data correspond to the cursor display position must be 0 state for the cursor display. When the 8'th line data is 1, the bit lights up regardless of the cursor existence.

3: The character pattern line positions correspond to the CG RAM data bits 0-4. As the CG RAM data bits 5-7 are not used for the display.

Note 4: When the character code bits 4-7 are all 0, the CG RAM character patterns are selected. As the character code bit 3 is an invalid bit, the character code Hex00 and Hex08 selects the same character pattern.

5: 1 : ON Data, 0 : OFF Data

b. In the case of 5 × 10 dots character patterns

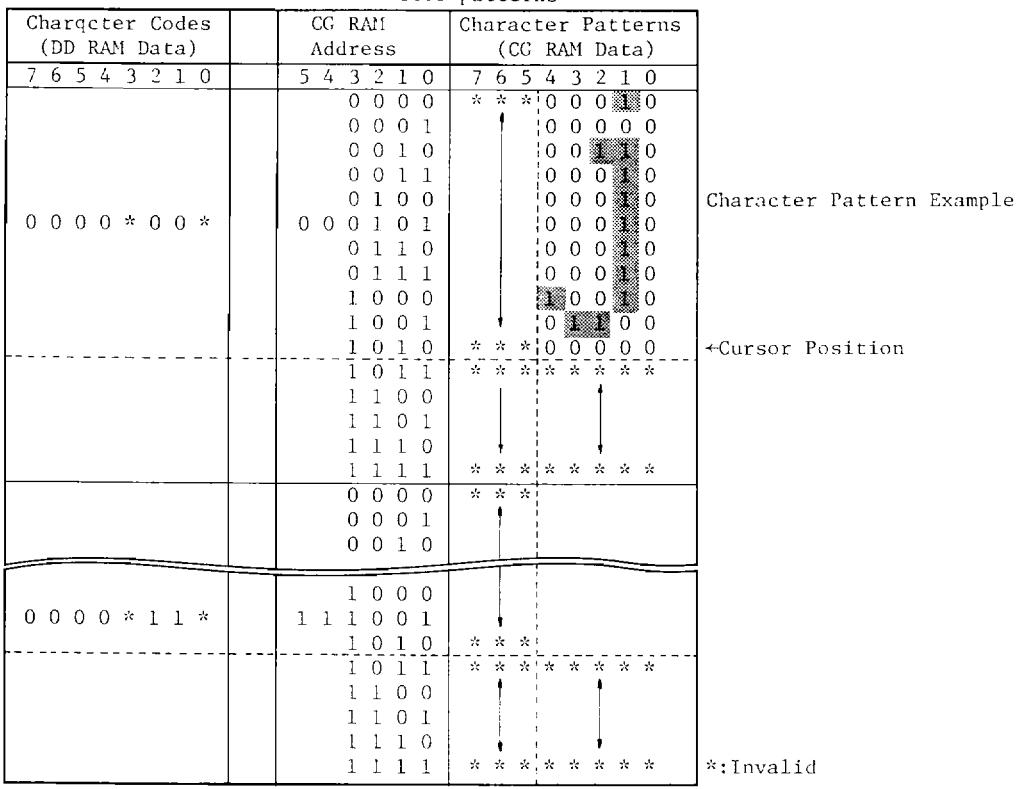


Fig. 4

Note 1: The character code bits 1 and 2 correspond to CG RAM address bits 4 and 5.

2: The CG RAM address bits 0-3 designate the character pattern line position. The 11'th line is in the cursor position and it is displayed in logical OR by the cursor. Therefore, the 11'th line data correspond to the cursor dispaly position must be 0 state for the cursor display.

When the 11'th line data is 1, the bit lights up regardless of the cursor existence. As the 12'th-16'th lines are not used for dispaly.

Note 3: When the character code bits 4-7 are all 0, the CG RAM character patterns are selected. As the character code bit 0 and 3 are invalid bit, character code Hex00,01,08 and 09 select the same character pattern.

4: 1 : ON Data, 0 : OFF Data

6. TIMING GENERATION CIRCUIT

The timing generation circuit is used to generate timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM.

It is designed so that the internal operation timing by MPU won't interfere with the internal operation timing by LCD display. Therefore, the data can be written from the MPU to DD RAM with no bad influence, for example, flickering in the areas other than the dispaly area where the data is written. This circuit is alsi used to generate timing signals to operate the external segment driver T6A92.

7. LCD DRIVER CIRCUIT

The LCD drive circuit consists of 16 common drivers and 50 segment drivers.

When the character font type and the number of lines are selected by the command, the valid common drivers automatically output drive waveforms, and other row drives output non-selection waveforms.

The character pattern data is sent serially through an internal 50 bit shift register, and latched when all needed data has sent. The segment drivers output drive waveforms corresponding to the latched datas.

8. SIGNALS FOR SEGMENT DRIVE WAVEFORMS

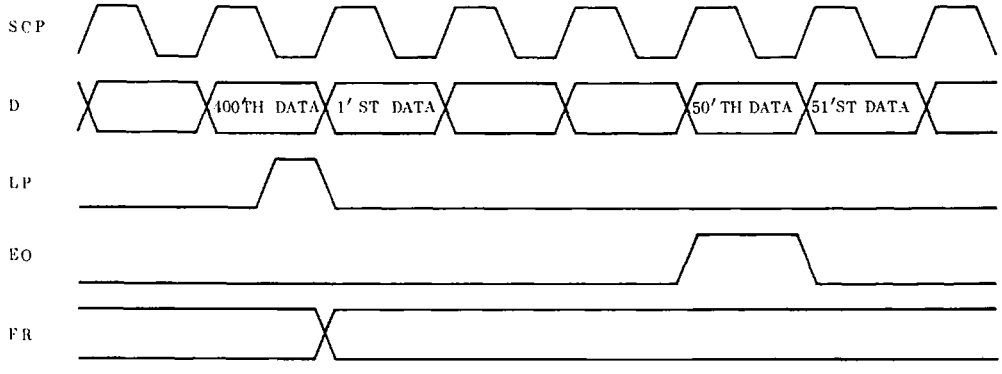


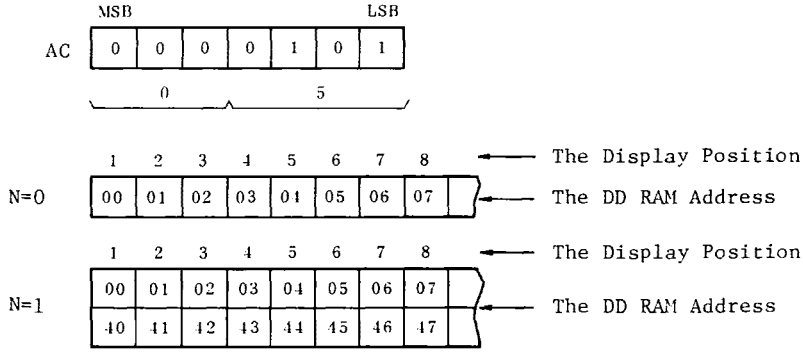
Fig. 5

Note: Fig.5 is in the 1-line dispaly mode.

9. CURSOR·BLINK CONTROL CIRCUIT

This circuit generates the cursor or blink. The cursor or blink appears in the digit corresponding to the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is Hex05 the cursor appears as shown below.



Note: The cursor or blink also appears when the character generator RAM (CG RAM) address is set in the address counter (AC). Therefore the cursor or blink appears regardless of the display data RAM (DD RAM) address.

10. RESET

A low signal on /RST terminal resets the T6A34. After being reset the T6A34 is automatically excuted the command (1)-(4). In the case of non-reset, excute the command (1)-(4) by the MPU.

(1) Display Clear

(2) Function Set ..... BL=1 : The blink is dispalyed by switching between all ON dots and the dispaly characters.
N=0 : 1-line dispaly
F=0 : 5 × 7 dots character font

(3) Entry Mode Set ..... I/D=1 : +1
S=0 : Non Shift

(4) Dispaly ON·OFF Control.. D=0 : Display OFF
C=0 : Cursor OFF
B=0 : Blink OFF

11. KEY MATRIX, LED CONTROL CIRCUIT

This control circuit is used to generate the key scan signals and the LED control signals. The key data that input to the SWC1-SWC8 are output from the SOD through a parallel-to-serial converter. The SWS1-SWS8 output the key scan signals and the LED data signals. The LE1-LE2 output the LED enable signals.

And the 2 × 8 LED matrix are composed of the LED data signals and the LED enable signals.

The key scan signals and the LED control signals are shown in Fig. 6.

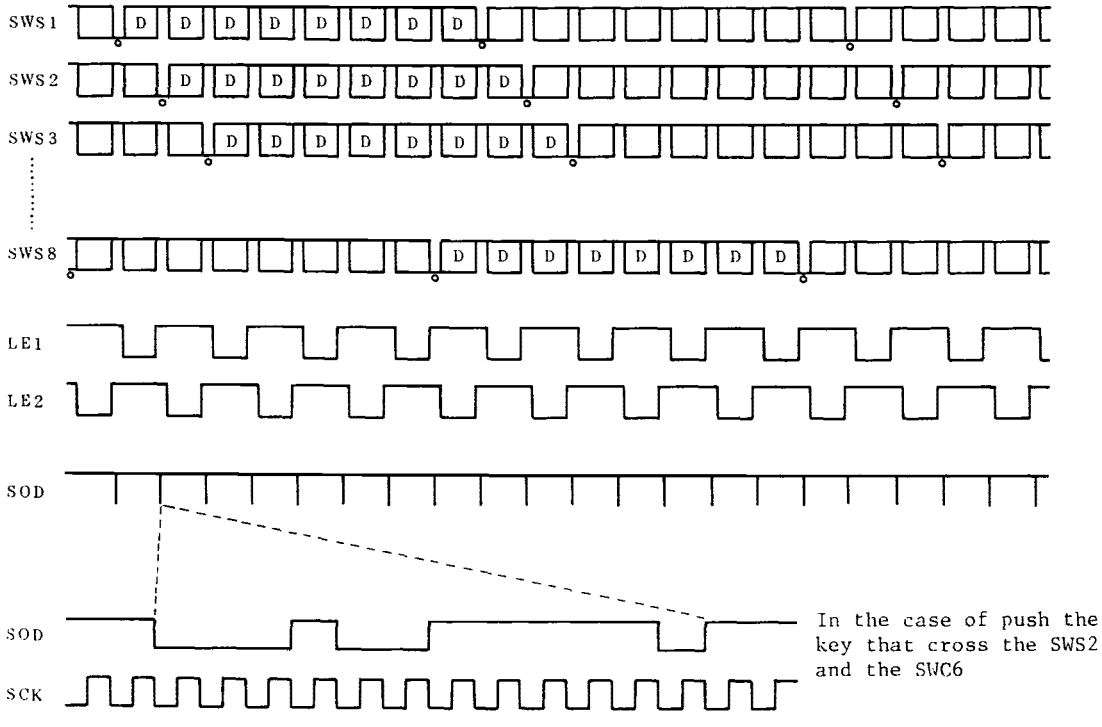


Fig. 6

Note: The symbol D stands for the LED control signal.
The symbol ° stands for the key scan signal.

The construction of 8×8 key scan matrix and 2×8 LED matrix is shown in Fig. 7.

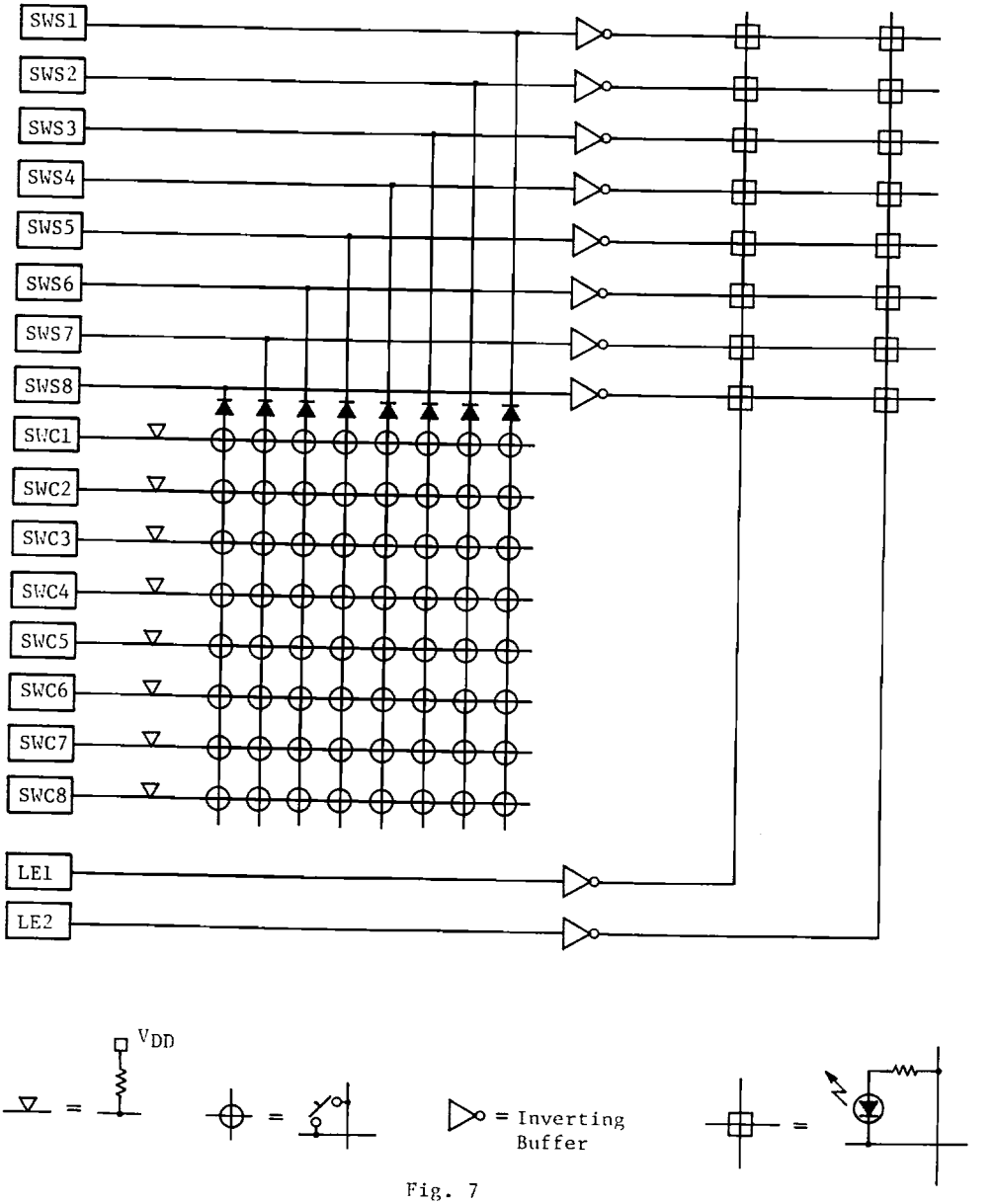
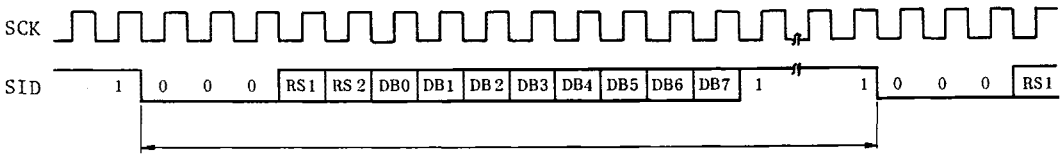


Fig. 7

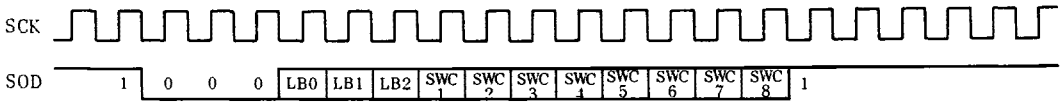
12. INPUT·OUTPUT DATA WAVEFORMS

(1) Input data waveform



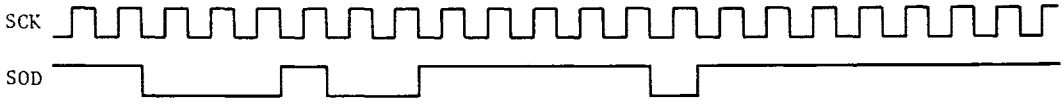
When the instruction of clear display and return home excuted: over 1.64ms
When the others instruction excuted: over 80μs

(2) Output data waveform



	LB0	LB1	LB2
SWS1	0	0	0
SWS2	1	0	0
SWS3	0	1	0
SWS4	1	1	0
SWS5	0	0	1
SWS6	1	0	1
SWS7	0	1	1
SWS8	1	1	1

In the case of push the key that cross the SWS2 and the SWC6

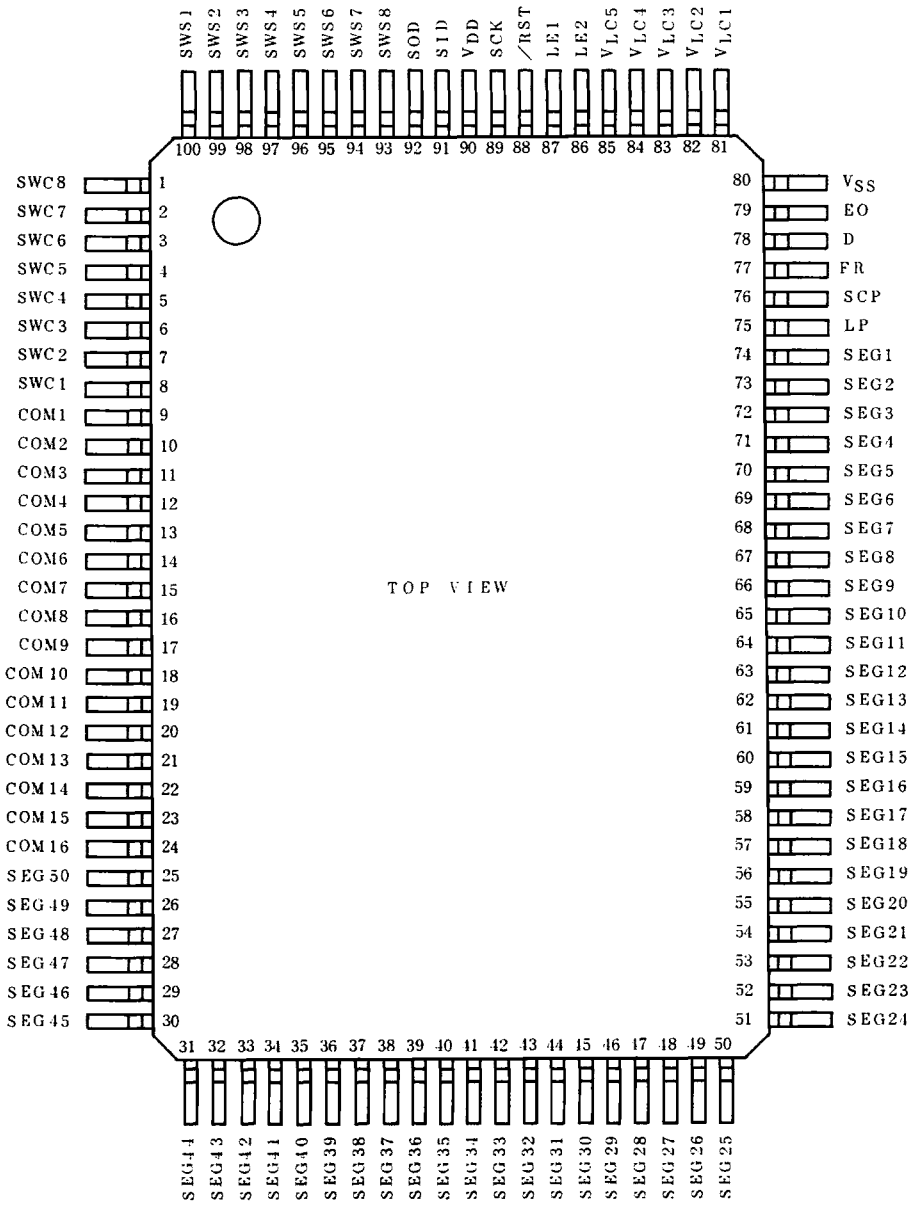


13. INSTRUCTION

The MPU can directly control only four registers. When an instruction is in process, none of the instructions are excuted. Therefore, after the before instruction is finished, excute the next instruction. In short, the MPU has to wait for an working time of the before instruction.

PIN FUNCTION

PIN CONFIGURATION



·PIN DESCRIPTION

PIN NAME	PIN No.	I/O	FUNCTION
SCK	89	I	Transmit Clock : This signal is used to synchronize SID and SOD.
SID	91	I	Transmit Data : Serial data input.
SOD	92	O	Transmit Data : Serial data output.
SWC1-SWC8	1-8	I	Key Matrix Inputs : SWC1-SWC8 which are connected to the SWS1-SWS8 through the 8×8 key matrix.
SWS1-SWS8	93-100	O	Key Matrix Outputs : SWS1-SWS8 which are used to scan the key matrix and control LED.
LP	75	O	Latch Pluse : This line transmits the latch signal to the segment driver T6A92.
SCP	76	O	Shift Clock Pluse : This signal is used to synchronize the serial data for the T6A92.
FR	77	O	Frame Pluse : This line transmits the switch signal to convert LCD wave from to A.C. to the T6A92.
D	78	O	Data : This transmits the display data to the T6A92.
EO	79	O	Enable Output : This line transmits the enable signal to the T6A92. A high on this pin enables the T6A92.
COM1-COM16	9-24	O	Common : Common driver outputs When 1/8 duty cycle selected, COM9-COM16 are disabled. When 1/11 duty cycle selected, COM12-COM16 are disabled.
SEG1-SEG50	25-74	O	Segment : Segment driver outputs.
V_{LC5}	87	I	Power supply pin for LCD drive.
V_{LC1}-V_{LC4}	83-86	I	Power supply pins for LCD drive.
V_{DD},V_{SS}	90,80	I	Power supply and ground pins. V_{DD}=5.0V±10%, V_{SS}=0V
/RST	88	I	Reset : Ahigh on this pin resets the T6A34.
LE1,LE2	81,82	O	LED Enable Outputs : LE1,LE2 which are connected to the SWS1-SWS8 through the 2×8 LED matrix.

FUNCTIONAL DESCRIPTION

•COMMAND EDFINITION

INSTRUCTION	CODE										DESCRIPTION	WORKING TIME f_{OSC}=250kHz (MAX.)
	RS1	RS2	D7	D6	D5	D4	D3	D2	D1	D0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear all display data and sets the DD RAM address Hex00.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets the DD RAM address Hex00 and return display to home position. The contents of the DD RAM don't change.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operation are executed, when data write.	40μs
Dispaly ON•OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON•OFF of all display (D). cursor ON•OFF (C), and blink of curosr position character (B).	40μs
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts scursor and display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	BL	N	F	T	*	Sets blink mode (BL), sets number of the display lines (N), character font (F), and test mode (T).	40μs

INSTRUCTION	CODE										DESCRIPTION	WORKING TIME f_{OSC}=250kHz (MAX.)
	RS1	RS2	D7	D6	D5	D4	D3	D2	D1	D0		
Set the CG RAM Address	0	0	0	1	CG RAM Address						Sets the CG RAM Address	40μs
Set the DD RAM Address	0	0	1	DD RAM Address							Sets the DD RAM Address	40μs
Data Write to the CG RAM or DD RAM	0	1	Write Data								Writes data into the CG RAM or DD RAM.	46μs
LED Data Write (1)	1	0	Write Data								Writes data into the LED data register(LER1)	0μs
LED Data Write (2)	1	1	Write Data								Writes data into the LED data register(LER2)	0μs

I/D=1: Increment
I/D=0: Decrement
S=1: Accompany display shift
S/C=1: Display Shift
S/C=0: Cursor Move
R/L=1: Shift to the right
R/L=0: Shift to the left
BL=1: The blink is displayed by switching between all ON dots and the display characters.
BL=0: The blink is displayed by switching between the display characters and the reverse ON·OFF of display characters.
N=1: 2 lines
N=0: 1 line
F=1: 5×10 dots
F=0: 5×7 dots
T=1: Enable test mode
T=0: Cancel test mode

1. CLEAR DISPLAY

	RS1	RS2	DB7	·····	DB0
Instruction Code	0	0	0	0	0	0	0	0	0	1

When this instruction is executed, the space code Hex 20 (Character pattern for character code Hex 20 must be blank pattern) is written into all the DD RAM address. The DD RAM address in the address counter is reset.
In other words, the display disappears and the cursor or blink goes to the left end (of the first line in the 2-line display mdoe). I/D of Entry mode is set (increment mode).
S of Entry mode doesn't change.

2. RETURN HOME

	RS1	RS2	DB7	·····	DB0	
Instruction Code	0	0	0	0	0	0	0	0	1	*	*:Invalid

When this instruction is executed, the DD RAM in the address counter is reset. When the display is shifted, it returns to its home position. The contents of DD RAM don't change.
The cursor or blink goes to the left end of the display (The left end of the first line in the 2-line display mode).

3. ENTRY MODE SET

	RS1	RS2	DB7	·····	DB0
Instruction Code	0	0	0	0	0	0	0	1	I/D	S

I/D : When a character code is written into the DD RAM, the DD RAM address is increased (I/D=1) or decreased (I/D=0) by 1.
When I/D=1, the cursor or blink moves to the right. When I/D=0 the cursor or blink moves to the left. The same applies to writing to the CG RAM.

S : When S=1 and I/D=1, the entire display shifts to the left at the time of writing to the DD RAM.
When S=1 and I/D=0, the entire display shifts to the right. Therefore, the cursor position looks as if it stands still and the display moves.
When S=0, the display doesn't shift.

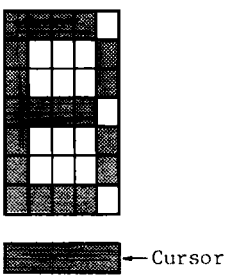
4. DISPLAY ON OFF CONTROL

	RS1	RS2	DB7	·····	DB0
Instruction Code	0	0	0	0	0	0	1	D	C	B

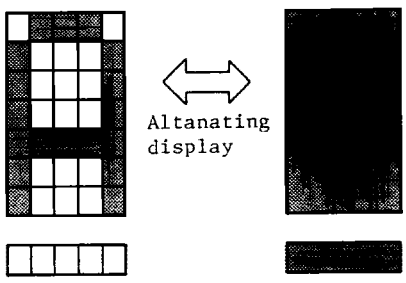
D : When D=1, the display is ON. When D=0, the display is OFF.
The DD RAM contents don't change even though D is reset. Therefore, it can be dispalyed as before by setting D.

C : When C=1, the cursor displayes. When C=0, the cursor doesn't display.
When the 5×7 dots character font is selected, the cursor is displayed using 5 dots in the 8'th line.
When the 5×10 dots character font is selected, the cursor is displayed using 5 dots in the 11'th line.

B : When B=1, the character corresponding to the cursor position blinks.
The blink is dispalyed by switching between all ON dots and the display characters or between the display characters and the reverse ON OFF of display characters. The cursor and the blink can be set to display simultaneously.
And when fcp=250kHz, the blink period is 409.6ms at 5×7 dots font mode or 563.2ms at 5×10 dots font mode.



(a) Cursor display example (5×7 dots)



(b) Blink display example (BL=1)

5. CURSOR DISPLAY SHIFT

	RS1	RS2	DB7	·····	DB0						
Instruction Code	0	0	0	0	0	1	S/C	R/L	*	*	*:Invalid

When this instruction is excuted, the cursor or display is shifted to the right or left without writing display data.

In the 2-lines display mode, the cursor is shifted from the 40'th digit of the 1'st digit of the 2'nd line displays shift at the same time, and only shift horizontally.

S/C	R/L	FUNCTION
0	0	Shift the cursor to the left.
0	1	Shift the cursor to the right.
1	0	Shift the all display to the left. The cursor follows the display shift.
1	1	Shift the all display to the right. The cursor follows the display shift.

When S/C=1, the address counter contents don't change.

6. FUNCTION SET

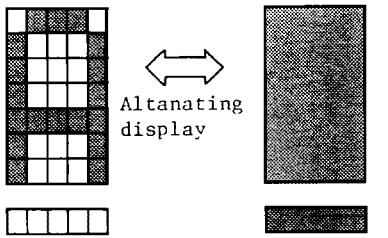
	RS1	RS2	DB7	·····	DB0					
Instruction Code	0	0	0	0	1	BL	N	F	T	*

*:Invalid

BL : When the BL=1, the blink is displayed by switching between the display characters and the reverse ON·OFF of display characters.
When the BL=0, the blink is displayed by switching between all ON dots and the display characters.

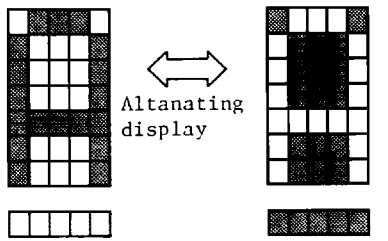
N : When the N=0, 1-line display mode is selected.
When the N=1, 2-lines display mode is selected.

F : When the F=0, 5×7 dots character font selected.
When the F=1, 5×10 dots character font selected.



(a) BL=1

N	F	Dispaly lines	Character font	Duty
0	0	1	5×7 dots	1/8
0	1	1	5×10 dots	1/11
1	*	2	5×7 dots	1/16

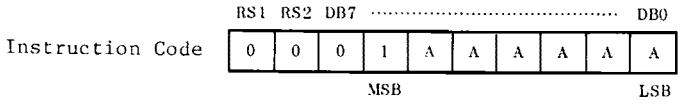


(b) BL=0

T : When the T=1, the test mode is selected.
Therefore, in case of this instruction is executed, sets in T=0.

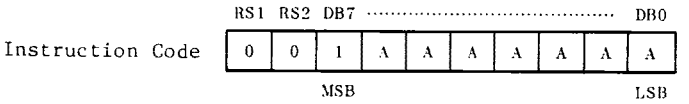
Note : Execute this instruction at the head of the program before executing all instructions.
After that time, this instruction can't be executed unless the blink mode is change.

7. CG RAM ADDRESS SET



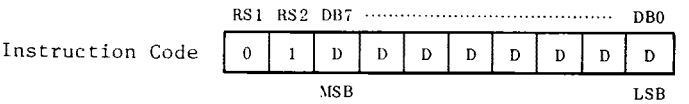
When this instruction is executed, the CG RAM address is set into the address counter in binary AAAAAA.

8. DD RAM ADDRESS SET



When this instruction is excuted, the DD RAM address is set into the address counter in binary AAAAAAA.

9. WRITE DATA TO DD RAM OR CG RAM



When this instruction is executed, the binary 8-bits data DDDDDDDD is written to the DD RAM or CG RAM.

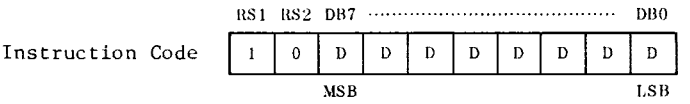
The previous instruction determines whether the data is writter to CG RAM or DD RAM.

Before executing the instruction, the CG RAM or DD RAM address set instruction must be executed.

After writing, the address is automatically increased by 1 according to the entry mode.

The display mode is also determined by the entry mode.

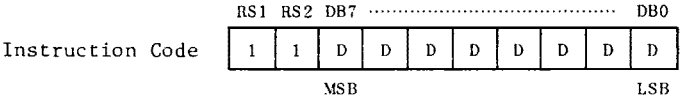
10. LED DATA WRITE (1)



When this instruction is executed, the binary 8-bits data DDDDDDDD is written to the LED data register(LER1).

And the eight LEDs that hold in common the LED enable signal LE1 are controlled.

11. LED DATA WRITE (2)



When this instruction is executed, the binary 8-bits data DDDDDDDD is written to the LED data register(LER2).

And the eight LEDs that hold in common the LED enable signal LE2 are controlled.

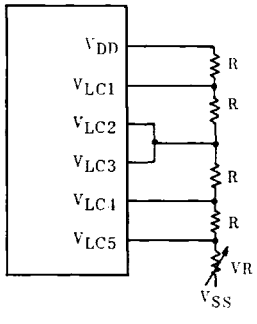
POWER SUPPLY FOR LCD DRIVE

Various voltage levels must be applied to the T6A34's terminals V_{LC1} to V_{LC5} to obtain the LCD drive waveforms.

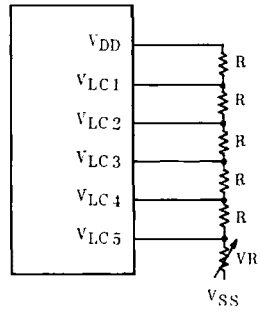
The voltage levels must be changed according to the duty factor. The following table shows the relation.

Power Supply \ Duty Factor / Bias	1/8, 1/11	1/16
	$\frac{1}{4}$	$\frac{1}{5}$
V_{LC1}	$V_{DD}-1/4V_{LCD}$	$V_{DD}-1/5V_{LCD}$
V_{LC2}	$V_{DD}-1/2V_{LCD}$	$V_{DD}-2/5V_{LCD}$
V_{LC3}	$V_{DD}-1/2V_{LCD}$	$V_{DD}-3/5V_{LCD}$
V_{LC4}	$V_{DD}-3/4V_{LCD}$	$V_{DD}-4/5V_{LCD}$
V_{LC5}	$V_{DD}-V_{LCD}$	$V_{DD}-V_{LCD}$

$V_{LCD}=V_{DD}-V_{LC5}$



(a) 1/e Bias

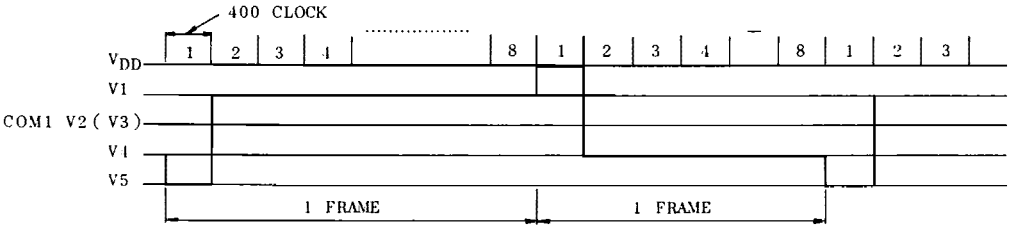


(b) 1/5 Bias

THE RELATION BETWEEN OSCILLATION FREQUENCY AND LCD FRAME FREQUENCY

The following examples of LCD frame frequency only apply when the oscillation frequency is 250kHz.

a. In case of 1/8 duty cycle



1 frame=4(μs)×400×8=12800(μs)=12.8(ms)

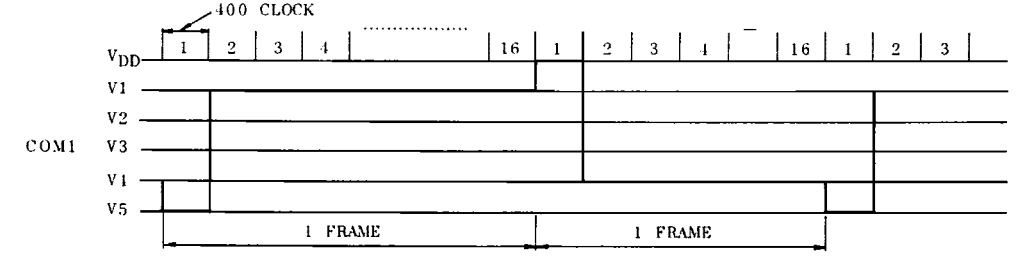
$$\text{frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

b. In case of 1/11 duty cycle

1 frame=4(μs)×400×11=17600(μs)=17.6(ms)

$$\text{frame frequency} = \frac{1}{17.6(\text{ms})} = 56.8(\text{Hz})$$

c. In case of 1/16 duty cycle



1 frame=4(μs)×200×16=12800(μs)=12.8(ms)

$$\text{frame frequency} = \frac{1}{12.8(\text{ms})} = 78.1(\text{Hz})$$

MAXIMUM RATINGS (Ta=25°C)

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT
Power Supply Voltage	V_{DD}		-0.3~7.0	V
Input Voltage	V_{IN}		-0.3~V_{DD}+0.3	V
Operating Temperature	T_{opr}		-20~75	°C
Storage Temperature	T_{stg}		-55~125	°C

Note 1: All voltage values are referenced to V_{SS}=0V

Note 2: Must maintain the following condition

$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5} \geqq V_{SS}$

(HIGH ← → LOW)

ELECTRICAL CHARACTERISTICS

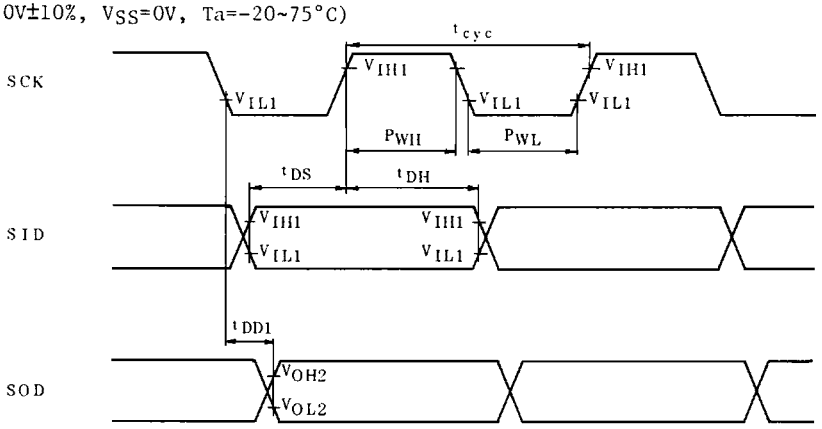
DC CHARACTERISTICS

(Unless otherwise specified, V_{DD}=5.0V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	PIN NAME
Operating Voltage 1	V_{DD}		4.5	-	5.5	V	
Operating Voltage 2	V_{LCD}	$V_{LCD}=V_{DD}-V_{LC5}$	3.0	-	V_{DD}	V	
Input High Voltage 1	V_{IH1}		V_{DD}-1.0	-	V_{DD}	V	SCK,DID,
Input Low Voltage 1	V_{IL1}		0	-	1.0	V	/RST
Hysterisis Voltage	V_H		-	0.7	-	V	SCK,SID,/RST
Input High Voltage 1	V_{IH2}		V_{DD}-1.2	-	V_{DD}	V	SWC1~SWC8
Input Low Voltage 2	V_{IL2}		0	-	1.9	V	
Output High Voltage 1	V_{OH1}	I_{OH}=-0.625mA	V_{DD}-0.3	-	-	V	D, SCP, LP,
Output Low Voltage 1	V_{OL1}	I_{OL}=0.625mA	-	-	0.3	V	EO, FR
Output High Voltage 2	V_{OH2}	I_{OH}=-1.6mA	2.4	-	-	V	SOD
		I_{OH}=-250μA	V_{DD}-0.8	-	-		
Output Low Voltage 2	V_{OL2}	I_{OL}=2.0mA	-	-	0.4	V	
Output High Voltage 3	V_{OH3}	I_{OH}=-250μA	V_{DD}-0.8	-	-	V	SWS1~SWS8
Output Low Voltage 3	V_{OL3}	I_{OL}=2.0mA	-	-	0.4	V	LE1,LE2
Row Driver On Resistance	R_{COM}	Id=±50μA	-	-	20	kΩ	COM1~16
Column Driver On Resistance	SEG	Id=±50μA	-	-	30	kΩ	SEG1~50
Input Leakage Current	I_{IL}	V_{IN}=0~V_{DD}	-	-	1	μA	SCK, SID
Power Supply Current	I_{DD}	All Outputs Open	-	-	800	μA	V_{DD}

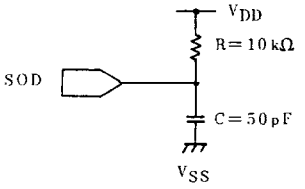
AC CHARACTERISTICS

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=-20~75°C)

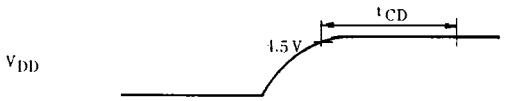


ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCK Cycle Time	t_{cyc}		2000	4000	8000	ns
SCK High Width	P_{WH}		$t_{cyc}/2-100$	-	-	ns
SCK Low Width	P_{WL}		$t_{cyc}/2-100$	-	-	ns
Data Set Up Time to SCK ↑	t_{DS}		50	-	-	ns
Data Hold Time from SCK ↑	t_{DH}		120	-	-	ns
Data Delay Time from SCK ↓						

A.C. Testing Load Circuit for SOD

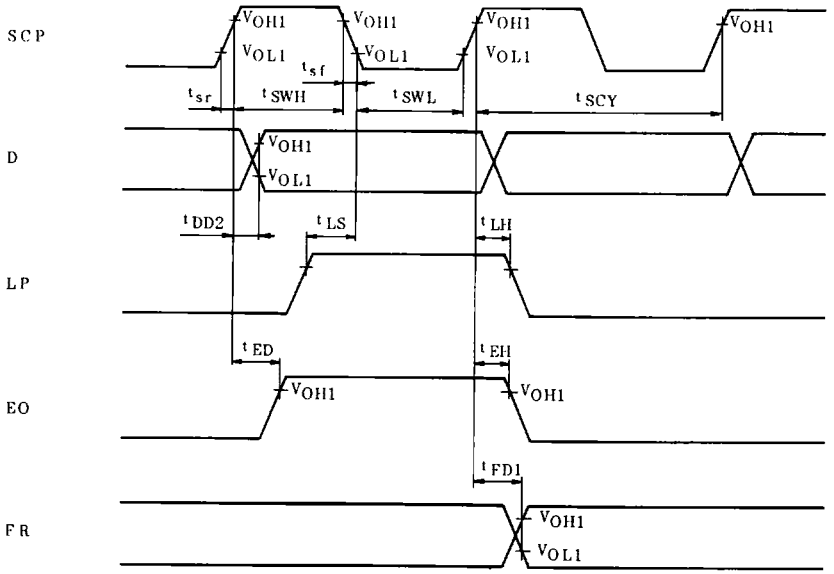


AT Power ON



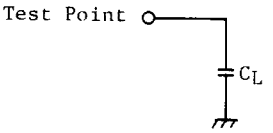
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Command Disable Time	t_{CD}		-	-	15	ms

.INTERFACE TIMING WITH THE SEGMENT DRIVER T6A92



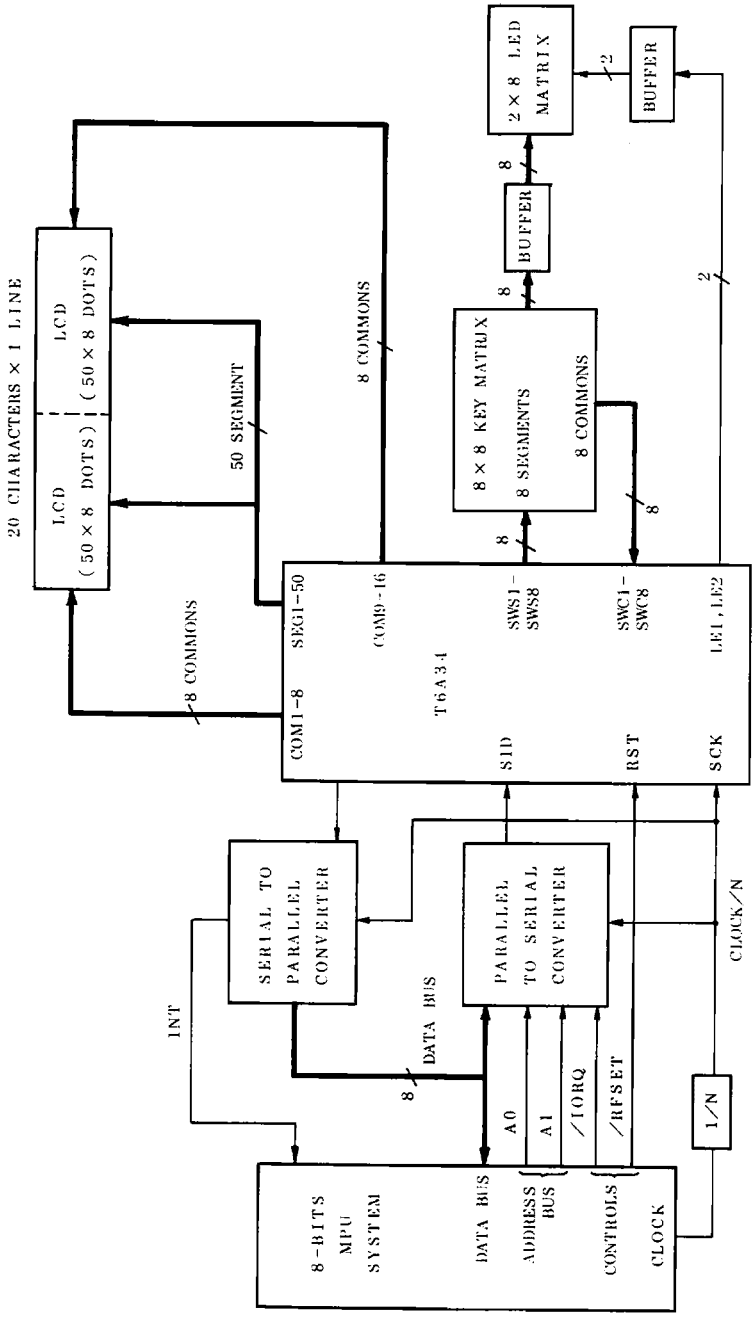
ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
SCP Cycle Time	t_{SCY}		2000	-	ns
SCP Pulse Width	$t_{SWH,L}$		800	-	ns
SCP Rise and Fall Time	t_{Sr}, t_{Sf}		-	100	ns
Data Delay from SCP ↑	t_{DD2}		-	100	ns
LP Set Up Time SCP ↓	t_{LS}		-120	0	ns
LP Hold Time from SCP ↑	t_{LH}		-100	0	ns
EO Delay Time from SCP ↑	t_{ED}		-	100	ns
EO Hold Time from SCP ↑	t_{EH}		-100	0	ns
FR Delay Time from SCP ↑	t_{FD1}		-100	100	ns

.A.C. TESTING LOAD CIRCUIT FOR INTERFACE TIMING

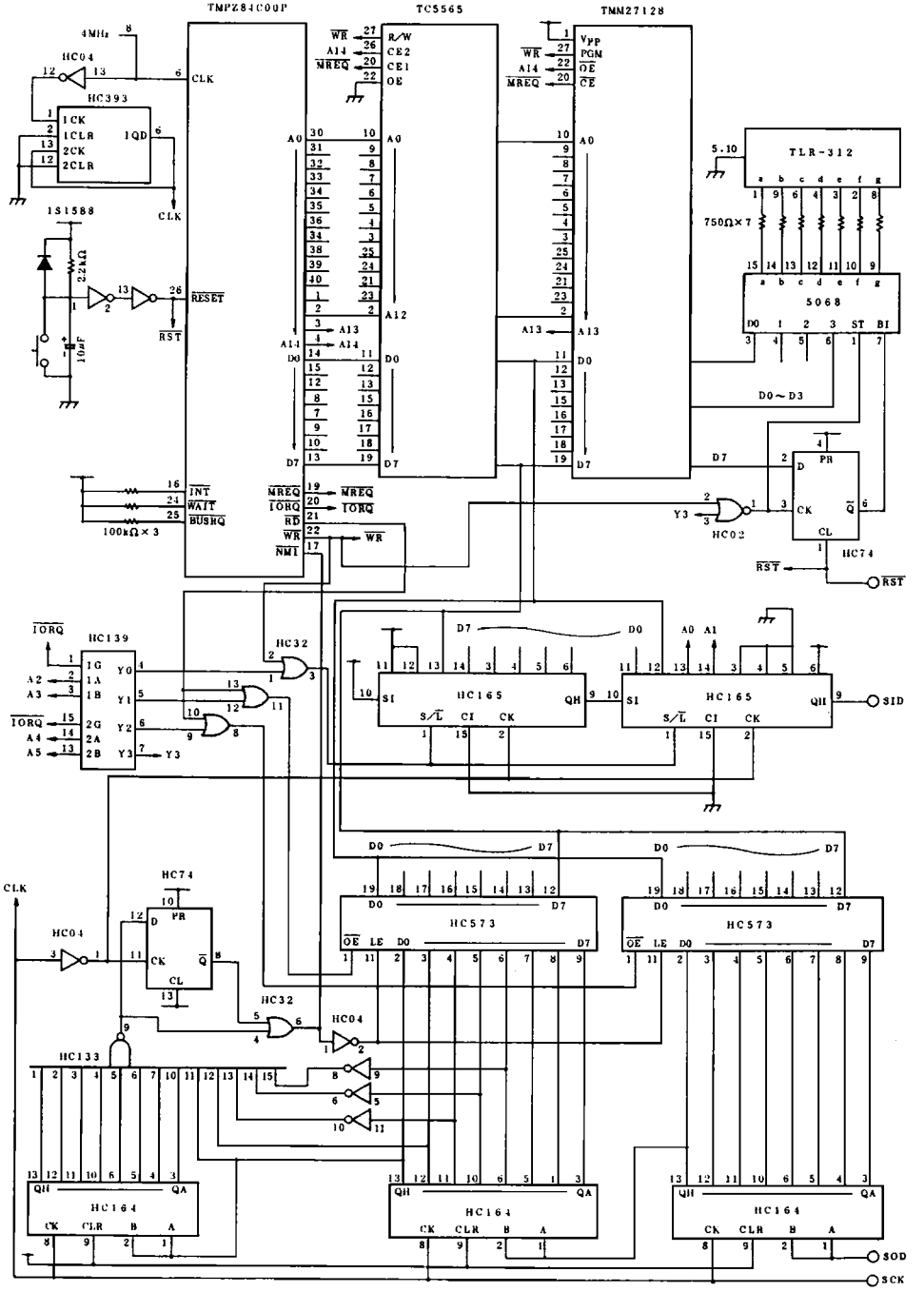


C_L=50pF

C_L includes jig capacitance


20 CHARACTERS × 1 LINE
LCD (50 × 8 DOTS)
LCD (50 × 8 DOTS)
50 SEGMENT
8 COMMONS
8 COMMONS
2 × 8 LED MATRIX
BUFFER
8 × 8 KEY MATRIX
8 SEGMENTS
8 COMMONS
BUFFER
COM1–8
SEG1–50
COM9–16
T6A34
SWS1–SWS8
SWC1–SWC8
LED1, LED2
SID
RST
SCK
SERIAL TO PARALLEL CONVERTER
PARALLEL TO SERIAL CONVERTER
INT
DATA BUS
CLOCK/N
1/N
8-BITS MPU SYSTEM
DATA BUS
ADDRESS BUS
CONTROLS
CLOCK
A0
A1
/IORQ
/RESET

APPLICATION-A



APPLICATION-B