

SANYO

No. 4349A

LC79431D**Dot Matrix LCD Driver**

Overview

The LC79431D is a large-scale dot matrix LCD common driver LSI. The LC79431D contains an 80-bit bidirectional shift register and a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the bit count. The LC79431D can be used in conjunction with segment driver LC79400D or LC79401D (QIP100D) to drive a wide-screen LCD panel.

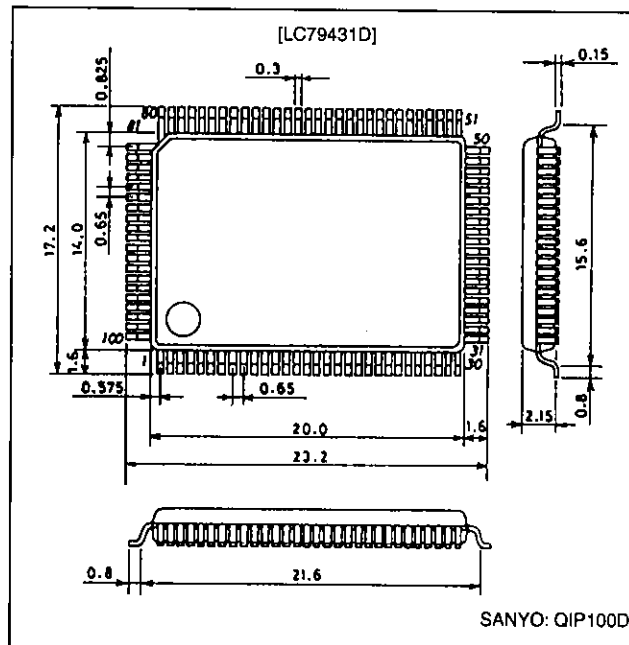
Features

- On-chip LCD drive circuit (80 bits)
- Display duty of 1/64 to 1/256 selectable
- On-chip input/output pins support a further increase in bit count
- Supports externally supplied bias voltage
- Operating supply voltage/operating temperature are:
 V_{DD} (logic block) : 5 V $\pm 10\%$ / -20 to $+75^\circ\text{C}$
 $V_{DD}-V_{EE}$ (LCD block) : 12 V to 32 V / -20 to $+75^\circ\text{C}$
- CMOS process

Package Dimensions

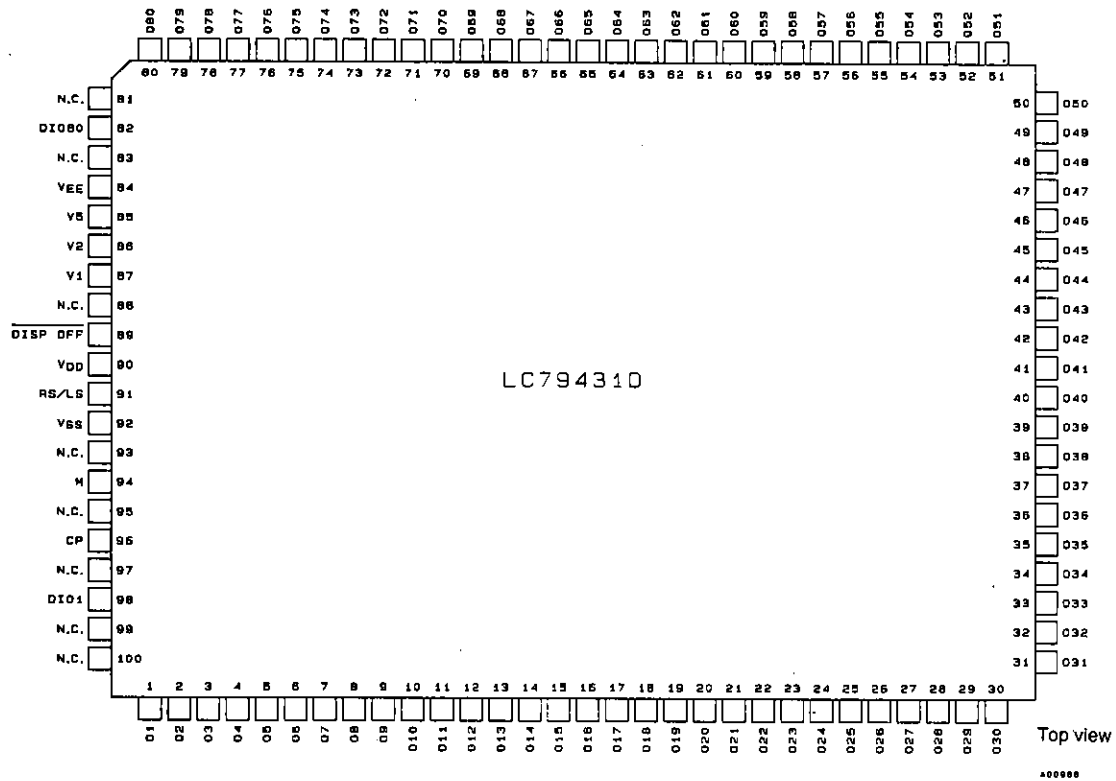
unit : mm

3180-QFP100D

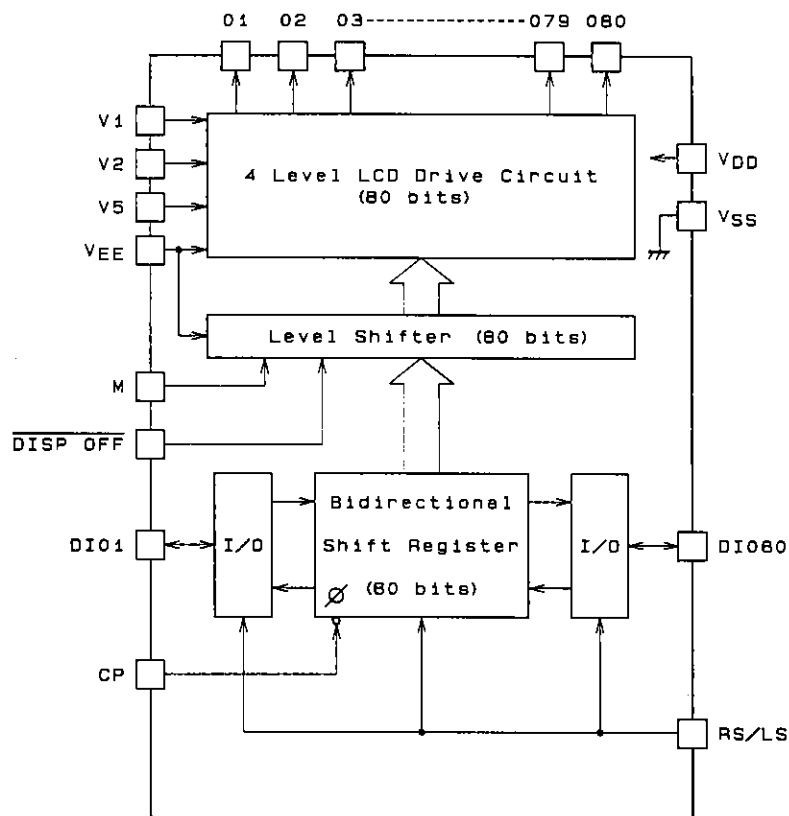


LC79431D

Pin Assignment



Equivalent Circuit Block Diagram



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Pin Descriptions

Pin No	Pin name	Input/Output	Functions																								
90	V _{DD}	Power supply	V _{DD} to V _{SS} : Power supply for logic block																								
92	V _{SS}																										
84	V _{EE}		V _{DD} to V _{EE} : Power supply for LCD drive block																								
87	V1	Power supply	LCD drive level power supply																								
86	V2		V1 to V _{EE} : Select level																								
85	V5		V2 to V5 : Nonselect level																								
96	CP	Input	Bidirectional shift register's shift clock (triggering on the trailing edge)																								
98	DIO1	Input/Output	<table><tr><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th></tr><tr><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td></tr><tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td></tr></table>	RS/LS	Data Transfer Direction	DIO1	DIO80	L (Shift right)	O1 → O80	IN	OUT	H (Shift left)	O80 → O1	OUT	IN												
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L (Shift right)	O1 → O80	IN		OUT																							
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82	DIO80	Input/Output																									
91	RS/LS	Input																									
94	M	Input	LCD drive output alternating signal																								
89	DISP OFF	Input	O1 to O80 output controlling input pin																								
1 ⋮ 80	O1 ⋮ O80	Output	LCD drive output The combination of scanning data, M signal, and $\overline{\text{DISP OFF}}$ signal can be used to create output levels as shown below. <table><tr><th>M</th><th>Data</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table> * Don't care (To be set to either "H" or "L")	M	Data	$\overline{\text{DISP OFF}}$	Output	L	L	H	V2	L	H	H	V _{EE}	H	L	H	V5	H	H	H	V1	*	*	L	V1
M	Data	$\overline{\text{DISP OFF}}$	Output																								
L	L	H	V2																								
L	H	H	V _{EE}																								
H	L	H	V5																								
H	H	H	V1																								
*	*	L	V1																								

Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

Parameter	Symbol	Ratings	Unit
Maximum supply voltage (logic)	V _{DD} max	-0.3 to +7.0	V
Maximum supply voltage (LCD)	V _{DD} -V _{EE} max *	0 to 35	V
Maximum input voltage	V _{IN} max	-0.3 to V _{DD} +0.3	V
Storage temperature range	T _{stg}	-40 to +125	°C

Note: * The voltages V1, V2, and V5 must obey the relationships: V_{DD} ≥ V1 > V2 > V5 > V_{EE}; V_{DD} - V2 ≤ 7V, V5 - V_{EE} ≤ 7V.

Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage (logic)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	$V_{DD}-V_{EE}$	*1, *2	12		32	V
Input high level voltage	V_{IH}	DIO1, DIO80, CP, M, RS/LS, DISP OFF	$0.8V_{DD}$			V
Input low level voltage	V_{IL}	DIO1, DIO80, CP, M, RS/LS, DISP OFF			$0.2V_{DD}$	V
CP (shift clock)	f_{CP}	CP			1	MHz
CP (pulse width)	t_{WC}	CP	63			ns
Setup time	t_{SETUP}	DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP,	100			ns
Hold time	t_{HOLD}	DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP,	100			ns
CP rise/fall time	t_R	CP			50	ns
	t_F	CP			50	ns

Note: 1. The voltages V_1 , V_2 , and V_5 must obey the relationships: $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} - V_2 \leq 7\text{V}$, $V_5 - V_{EE} \leq 7\text{V}$.

2. When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

Electrical Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 5\text{V} \pm 10\%$

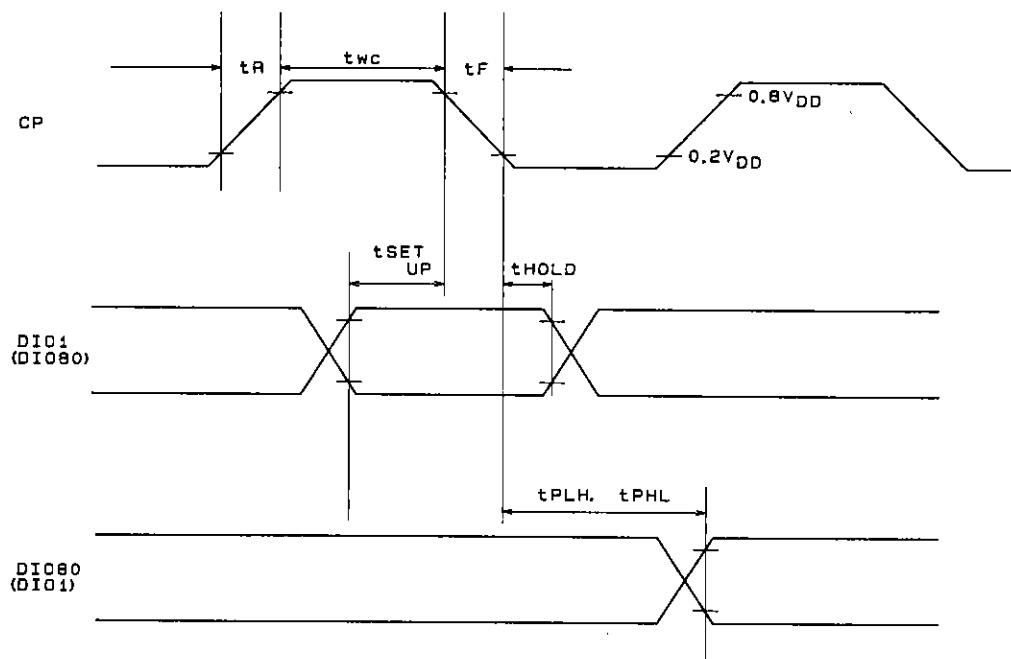
Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	I_{IH}	$V_{IN} = V_{DD}$, $V_{DD} = 5.5\text{V}$; DIO1, DIO80, CP, M, RS/LS, DISP OFF			1	μA
Input low level current	I_{IL}	$V_{IN} = V_{SS}$, $V_{DD} = 5.5\text{V}$; DIO1, DIO80, CP, M, RS/LS, DISP OFF	-1			μA
Output high level voltage	V_{OH}	$I_{OH} = -0.4\text{mA}$, $V_{DD} = 4.5\text{V}$; DIO1, DIO80	$V_{DD}-0.4$			V
Output low level voltage	V_{OL}	$I_{OL} = 0.4\text{mA}$, $V_{DD} = 4.5\text{V}$; DIO1, DIO80			0.4	V
Drive-on resistor	$R_{ON}(1)$	$V_{DD}-V_{EE} = 30\text{V}$, $ V_{DE}-V_0 = 0.5\text{V}$ $V_{DD} = 4.5\text{V}$ *; O1 to O80			1.0	$\text{k}\Omega$
	$R_{ON}(2)$	$V_V-V_{EE} = 20\text{V}$, $ V_{DE}-V_0 = 0.5\text{V}$, $V_{DD} = 4.5\text{V}$ *; O1 to O80			1.0	$\text{k}\Omega$
Current drain (1)	I_{SS}	$V_{DD}-V_{EE} = 30\text{V}$, CP = 14 kHz, no load, $V_{DD} = 5.5\text{V}$; V_{SS}			100	μA
Current drain (2)	I_{EE}	$V_{DD}-V_{EE} = 30\text{V}$, CP = 14 kHz, no load, $V_{DD} = 5.5\text{V}$; V_{EE}			100	μA
Input capacitance	C_I	$f = 1\text{MHz}$; CP		5		pF

Note: * $V_{DE} = V_1$ or V_2 or V_5 or V_{EE} $V_1 = V_{DD}$, $V_2 = 16/17 (V_{DD}-V_{EE})$, $V_5 = 1/17 (V_{DD}-V_{EE})$

Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{DD} = 5\text{V} \pm 10\%$

Parameter	Symbol	Conditions	min	typ	max	Unit
Output delay time	t_{PLH}	$C_L = 15\text{pF}$; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80			250	ns
	t_{PHL}	$C_L = 15\text{pF}$; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80			250	ns

Switching Characteristics Diagram



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