NEC

MOS INTEGRATED CIRCUIT

μPD3753

2088-BIT CCD LINEAR IMAGE SENSOR WITH PERIPHERAL CIRCUIT

The μPD3753 is a 2088-bit high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3753 consists of 2088-bit photocell array and a line of 2088-bit CCD charge transferred register. It contains a reset a feed-through level clamp circuit, a pulse generator, and a voltage amplifier to provide high sensitivity and low noise. It also supports low power consumption with single 5 V power supply. The μPD3753 can be driven by power supply and three input clocks owing to the built-in reset pulse generator and a clamp pulse generator.

FEATURES

- Valid photocell : 2088-bit
- Photocell's pitch : 14 μm
- High response sensitivity : Providing a response equal with the existing equivalent NEC product (μPD3743) to the light from a daylight fluorescent lamp
- Low noise : Providing about two thirds register imbalance of the existing equivalent NEC product (μPD3743)
- Peak response wavelength : 550 nm (green)
- Resolution : 8 dot/mm across the shorter side of a B4-size (257 × 364 mm) sheet
- Power supply : +5 V
- Drive clock level : CMOS output under +5 V operation
- Scanning speed : 1.0 ms/line
- Built-in circuit : Reset feed-through level clamp circuit, reset pulse generator, clamp pulse generator

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD3753CY	CCD LINEAR IMAGE SENSOR 22 PIN PLASTIC DIP (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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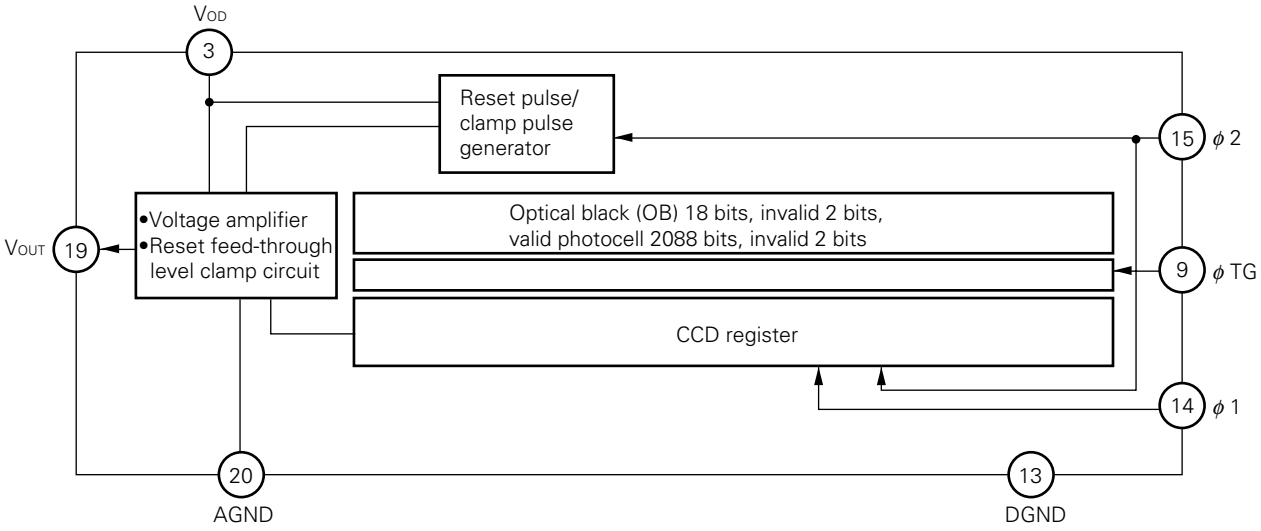
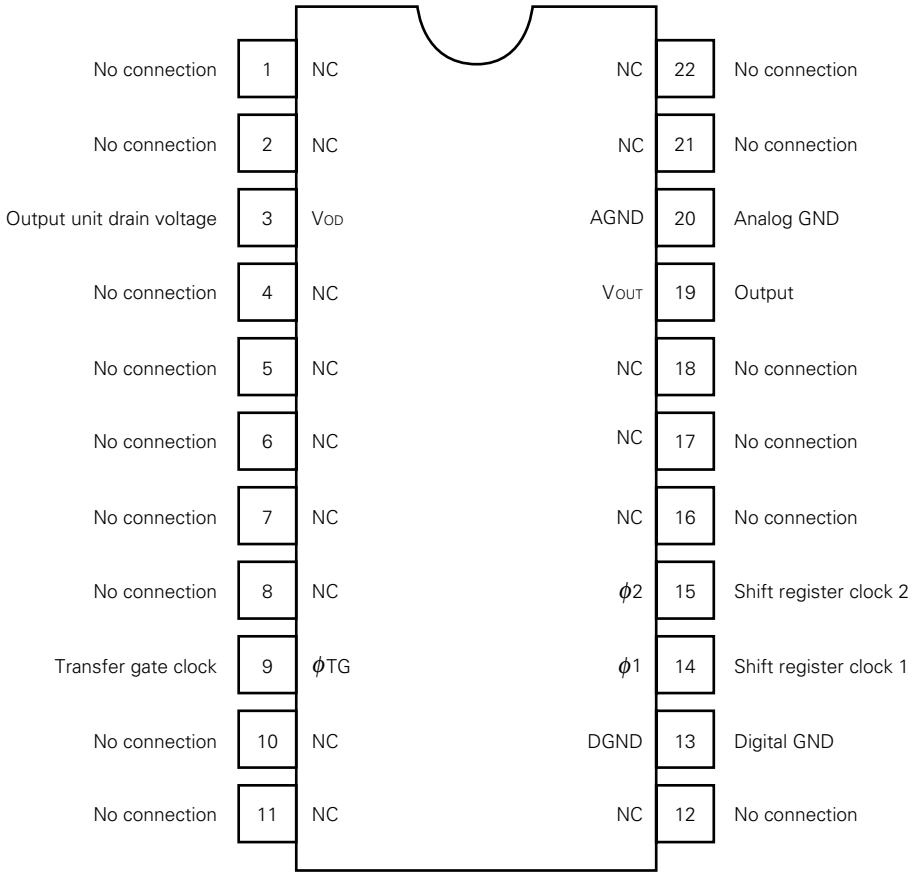
BLOCK DIAGRAM

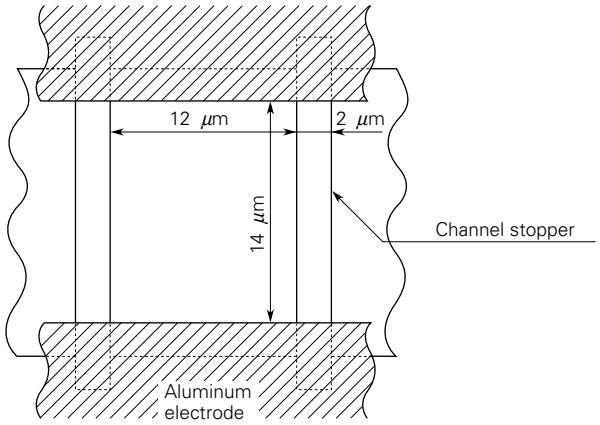


PIN CONFIGURATION (Top View)

CCD LINEAR IMAGE SENSOR 22 PIN PLASTIC DIP (400 mil)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output unit drain voltage	V_{OD}	–0.3 to +8	V
Shift register clock voltage	$V_{\phi1, \phi2}$	–0.3 to +8	V
Transfer gate signal voltage	$V_{\phi TG}$	–0.3 to +8	V
Operating ambient temperature	T_{opt}	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +70	°C

RECOMMENDED OPERATING CONDITIONS (T_a = –25 to + 60 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V_{OD}	4.7	5.0	5.3	V
Shift register clock $\phi1$, $\phi2$ signal high level	$V_{\phi1H, \phi2H}$	4.5	5.0	V_{OD} + 0.2	V
Shift register clock $\phi1$, $\phi2$ signal low level	$V_{\phi1L, \phi2L}$	–0.3	0	+0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	$V_{\phi1H}$	$V_{\phi1H}$	V
Transfer gate signal low level	$V_{\phi TGL}$	–0.3	0	+0.5	V
Data rate	$f_{\phi R}$	0.2	1	2	MHz

Caution When $V_{\phi TGH} > V_{\phi1H}$, image lag increases.

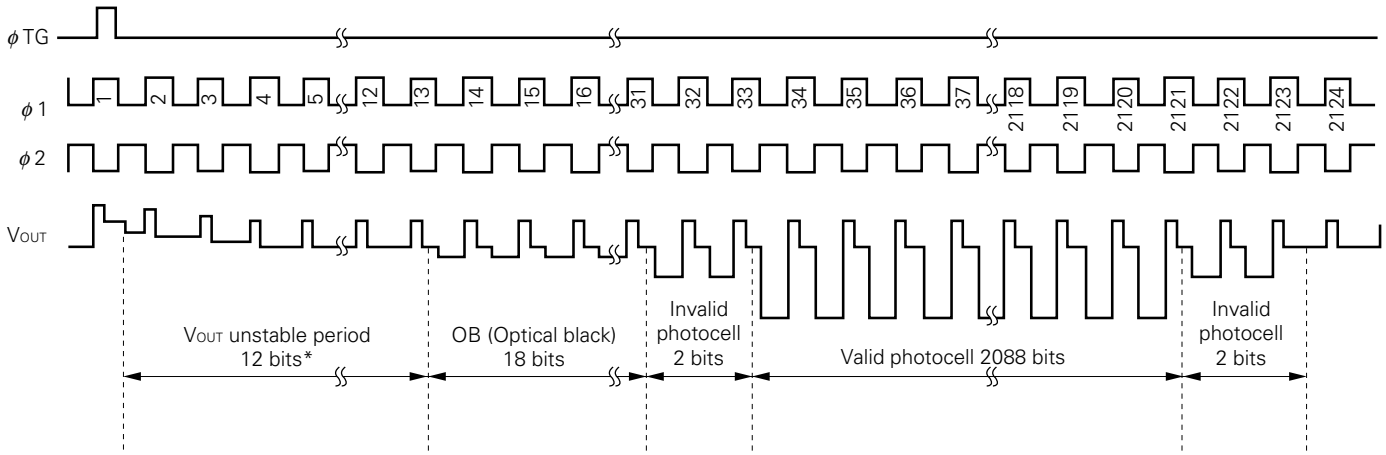
ELECTRICAL CHARACTERISTICS

(T_a = +25 °C, V_{OD} = 5 V, $f\phi_1$ = 1 MHz, data rate = 1 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C500 (infrared cut filter), input clock = 5 V_{P-P})

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.0	1.2		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.013		lx·s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		± 2	± 8	%
Average dark signal	ADS	Light shielding		1.0	8.0	mV
Dark signal non-uniformity	DSNU	Light shielding	– 8	± 4	+ 8	mV
Power consumption	P_W			30	50	mW
Output impedance	Z_O			0.5	1	kΩ
Response	R_F	Daylight color fluorescent lamp	63	90	117	V/lx·s
Response peak wavelength				550		nm
Image lag	IL	V_{OUT} = 1 V		7	14	%
Offset level	V_{OS}		2.5	3.0	3.5	V
Input capacitance of shift register clock pin	$C\phi_1$ $C\phi_2$			300		pF
Input capacitance of transfer gate signal pin	$C\phi_{TG}$			100		pF
Output fall delay time	t_d			130		ns
Total transfer efficiency	TTE	V_{OUT} = 1 V, data rate = 2 MHz	92			%
Dynamic range	DR	V_{sat}/DSNU		375		times
Reset feed-through noise	RFSN	Light shielding	0	800	1500	mV
Bit noise	BN	Light shielding		10		mV_{P-P}
Resolution	MTF	Modulation transfer function at nyquist frequency		65		%

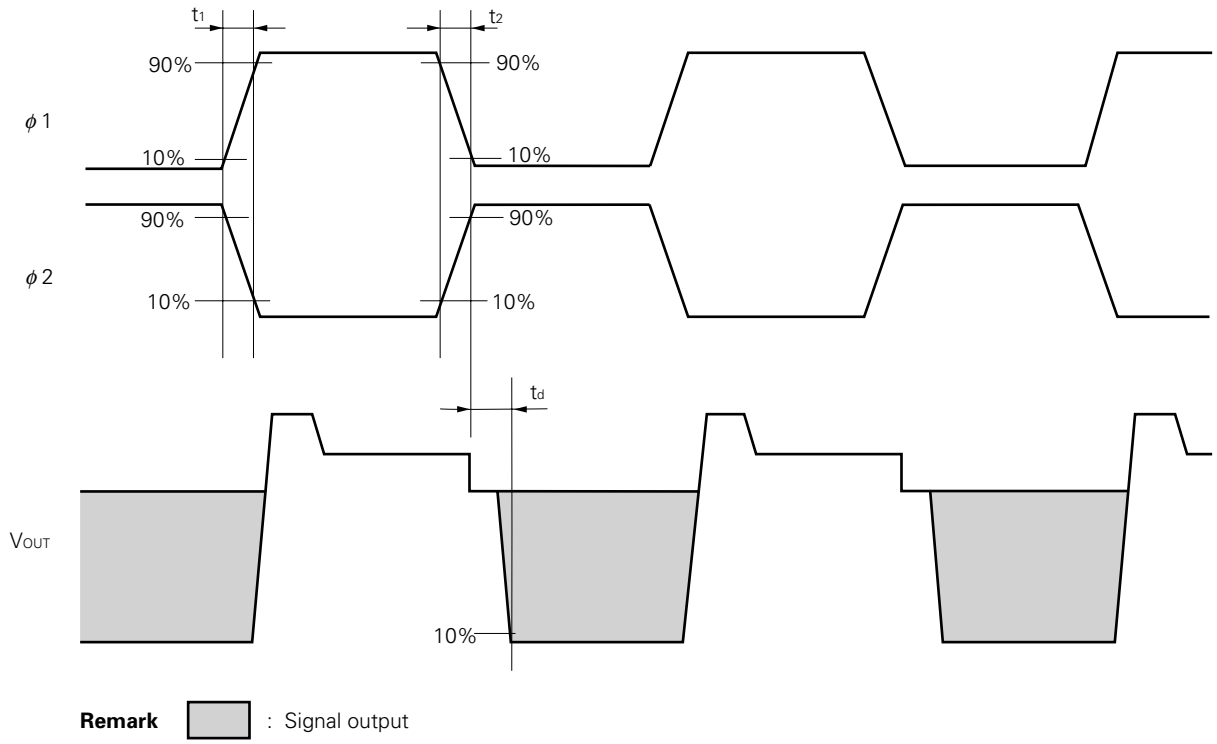
Remark When V_{OD} = 4.7 V, the response typically decreases to 90 % of the value under 5 V operation.

TIMING CHART 1



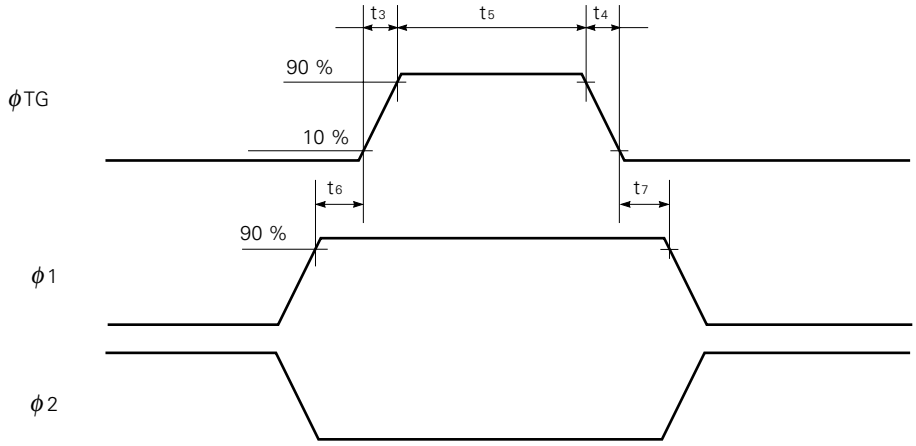
Caution Be sure not to use this period (indicated by *) as the black level, because this part is unstable.

TIMING CHART 2

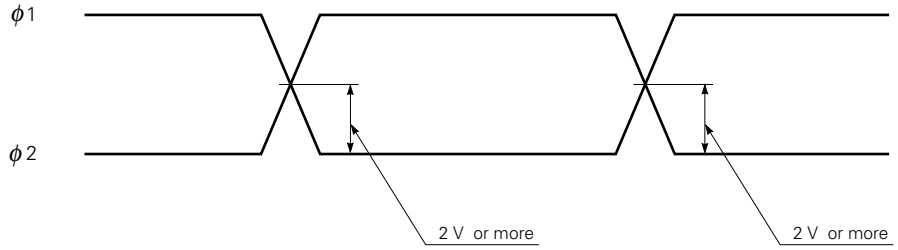


Remark : Signal output

TIMING CHART for ϕTG, ϕ1, ϕ2



CROSS POINTS for ϕ1, ϕ2



Note Adjust cross point of ϕ1, ϕ2 by ϕ1, ϕ2 pin external input resistors.

(Unit: ns)

Parameter	MIN.	TYP.	MAX.
t_1 , t_2	0	50	(100)
t_3, t_4	0	50	–
t_5	650	1000	(2000)
t_6, t_7	0	100	–

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD3753 is destroyed.

DEFINITIONS OF CHARACTERISTIC ITEMS

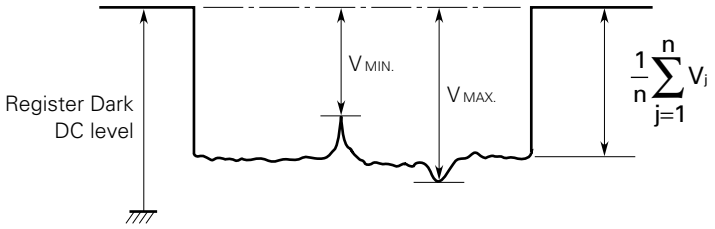
1. Saturation voltage: V_{sat}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU\ (\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

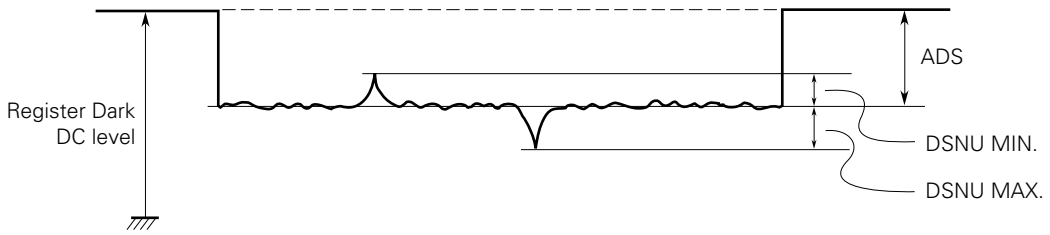
n : Number of valid bits
V_j : Output voltage of each bit



4. Average dark signal: ADS
   Output average voltage in light shielding.

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

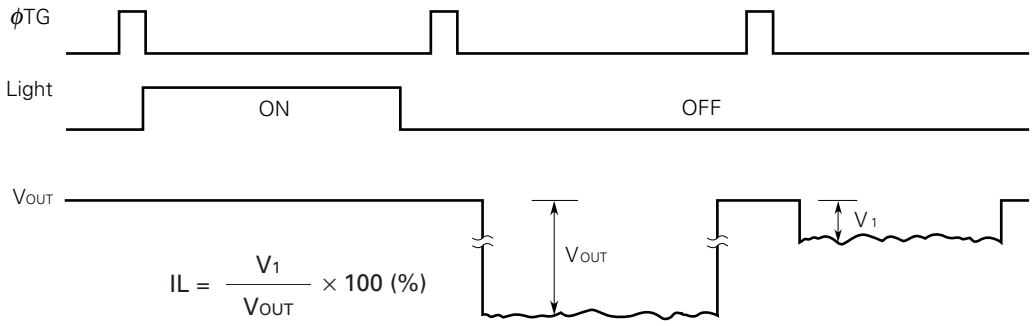
5. Dark signal non-uniformity: DSNU
   The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Z_o
   Output pin impedance viewed from outside.

7. Response: R
   Output voltage divided by exposure (lx·s).
   Note that the response varies with the light source.

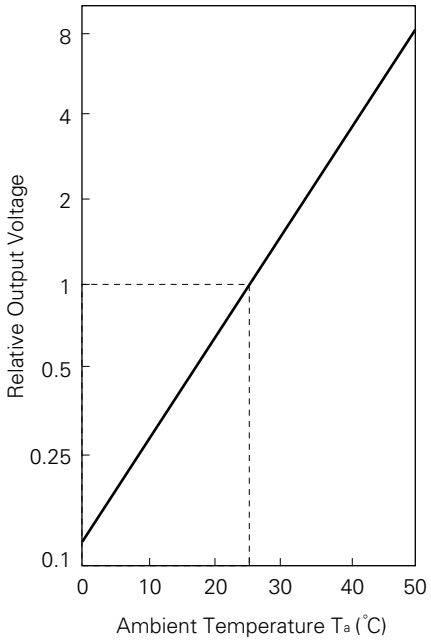
8. Image Lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.



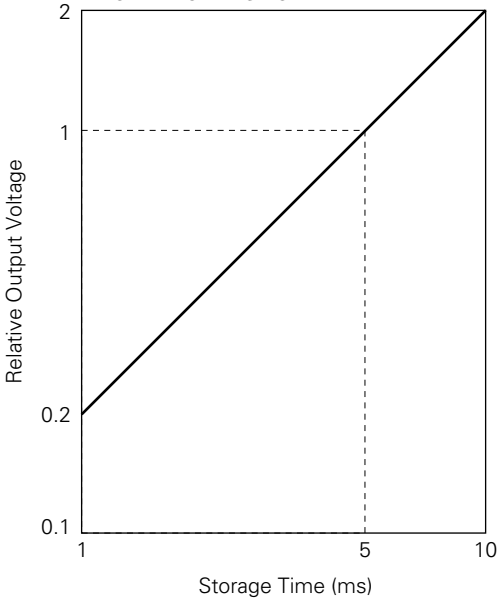
9. Bit Noise: BN
   Output signal distribution of a photocell by scan.

STANDARD CHARACTERISTIC CURVES (T_a = +25 °C)

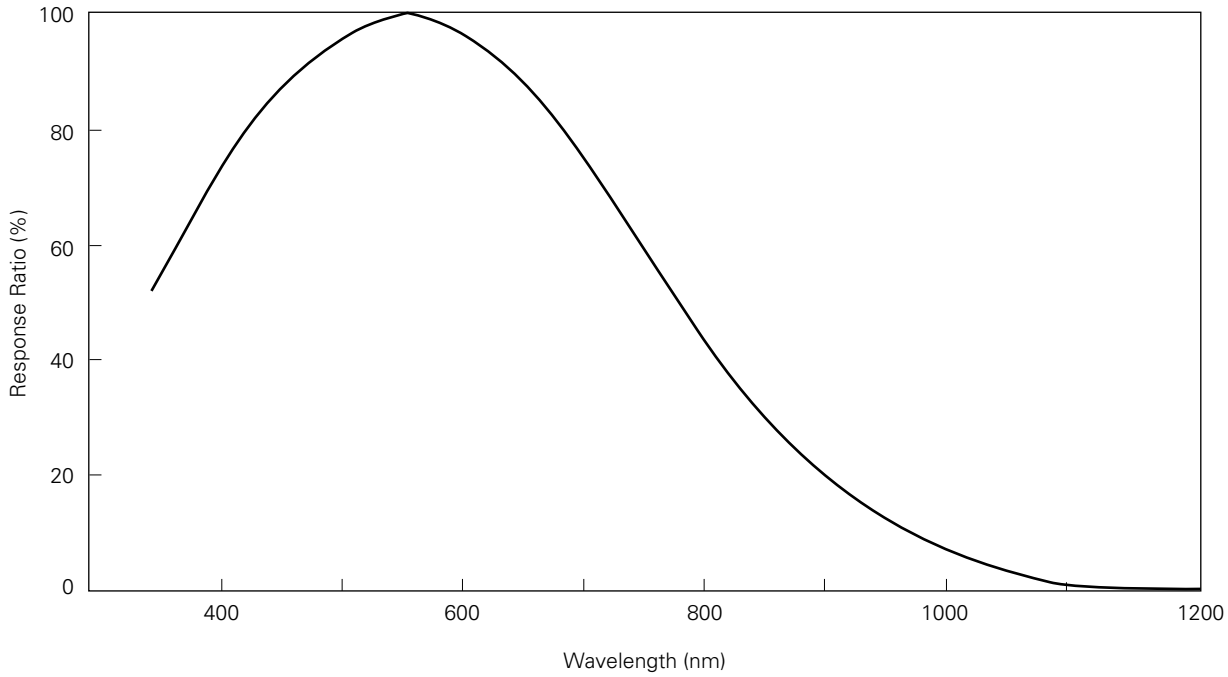
DARK OUTPUT TEMPERATURE CHARACTERISTIC



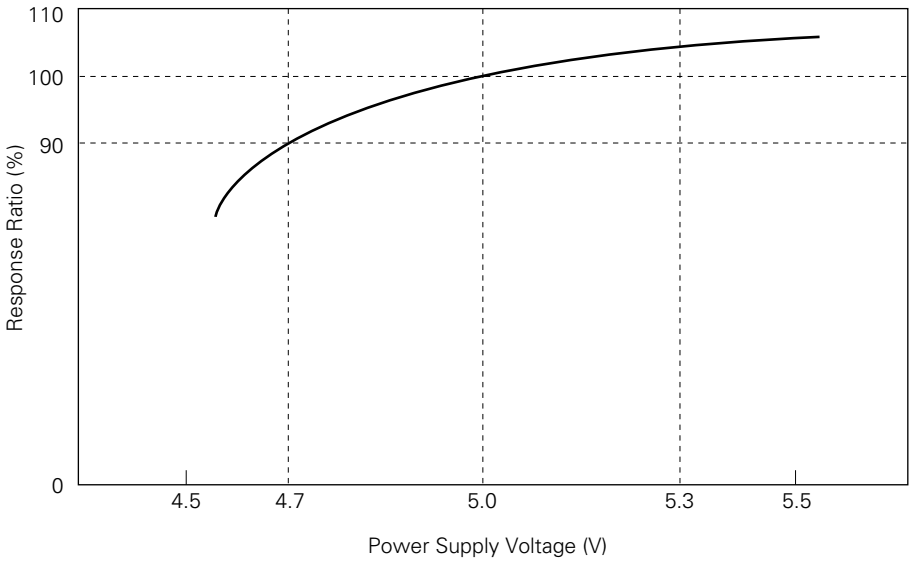
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC



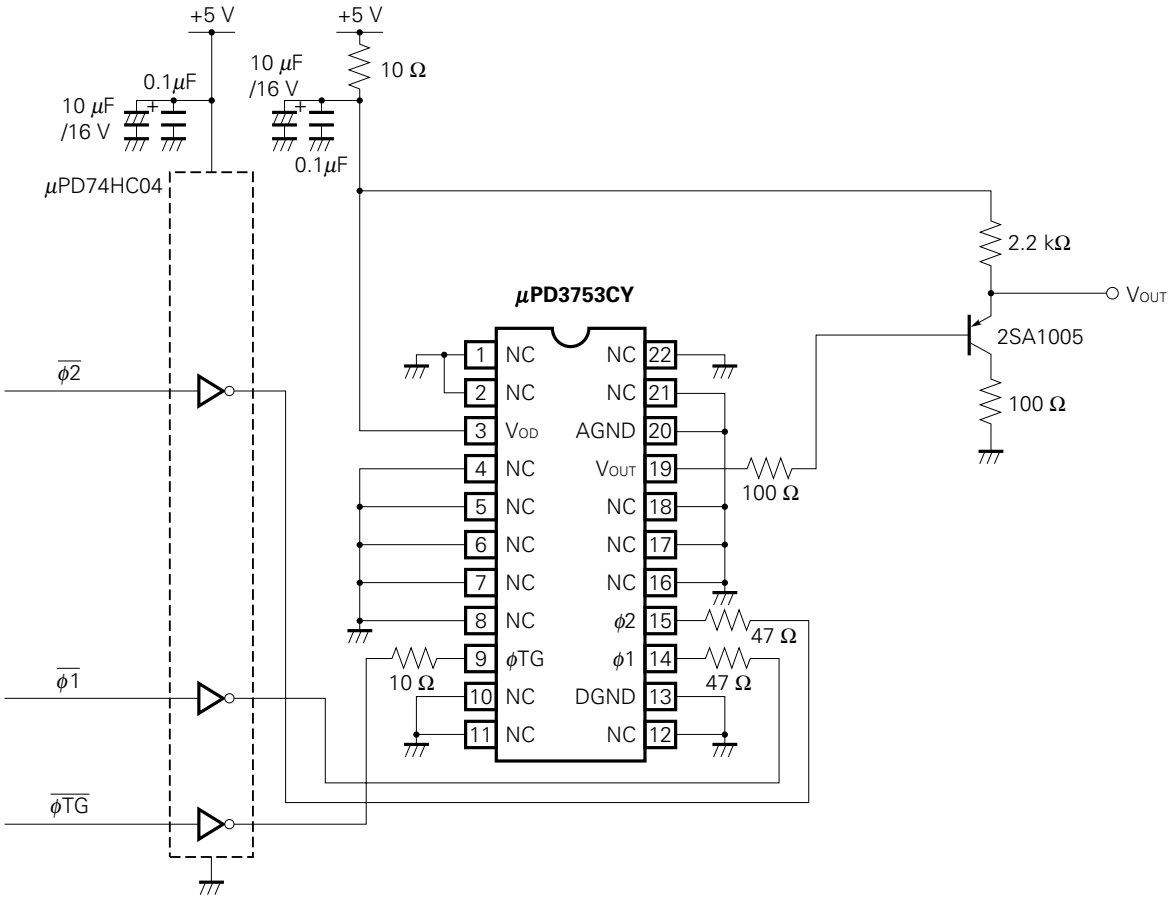
SPECTRAL RESPONSE CHARACTERISTIC



POWER SUPPLY VOLTAGE RESPONSE RATIO CHARACTERISTIC



APPLICATION EXAMPLE

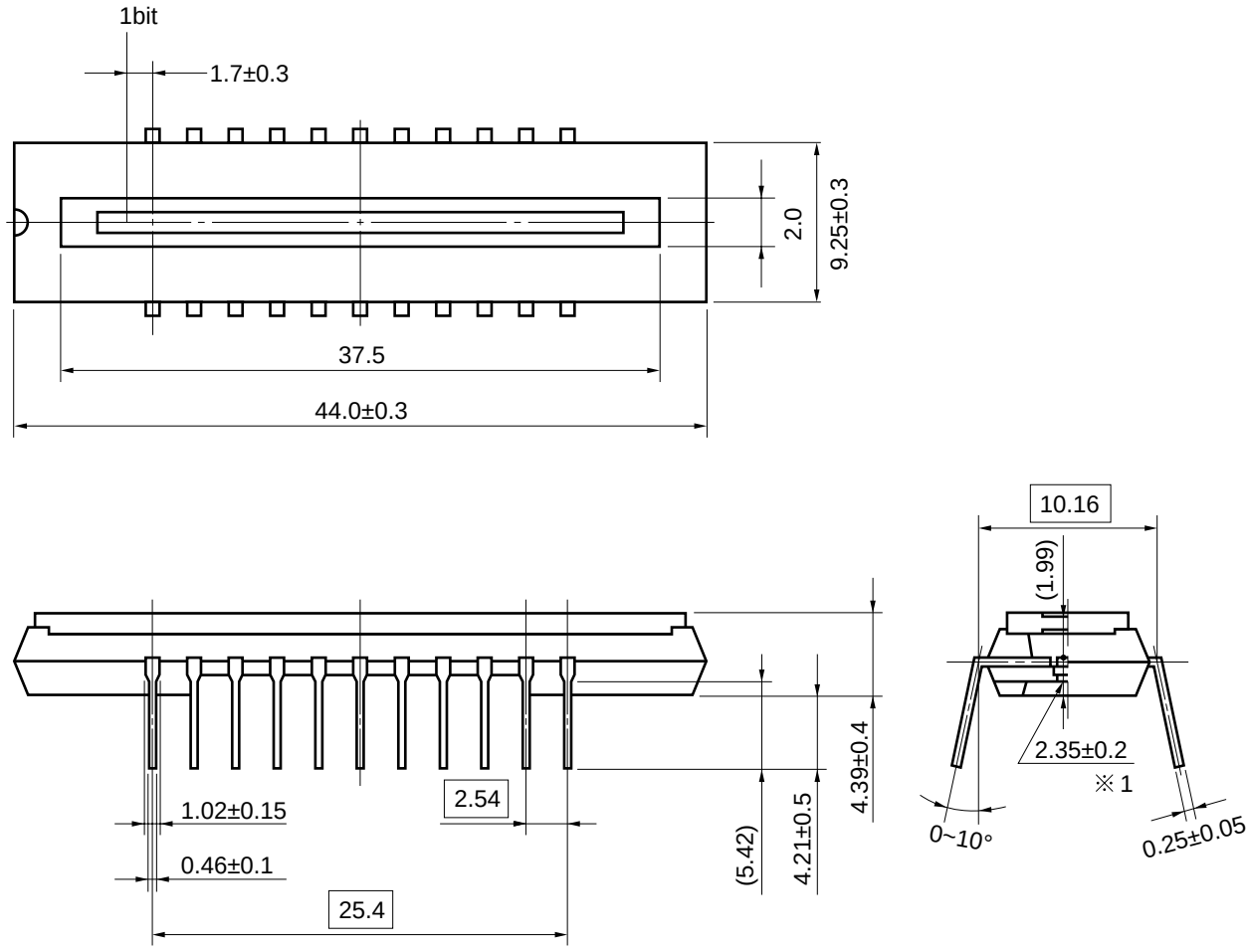


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS

CCD LINEAR IMAGE SENSOR 22PIN PLASTIC DIP (400 mil)

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	$42.9 \times 8.35 \times 0.7$ ※2	1.5

※1 The bottom of the package ⟷ The surface of the chip

※2 The thickness of the cap over the chip

22C-1CCD-PKG2

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 1 Type of Through Hole Device

μPD3753CY: CCD LINEAR IMAGE SENSOR 22 PIN PLASTIC DIP (400 mil)

Soldering Process	Soldering Conditions
Wave soldering (Only lead part)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 260 °C or below, Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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