Calculators



MM5766 calculator programmer

general description

The MM5766 provides a convenient and inexpensive means of adding "learn mode" programmability to the National Semiconductor MM5758 scientific calculator chip. The monolithic MOS integrated circuit combines P-channel enhancement and depletion mode technologies to obtain low voltage and low power characteristics necessary for economical battery-powered products.

The MM5766 is a dynamic key sequence programmer that memorizes any combination of key entries while in the Load Mode, then automatically plays back the programmed sequence as often as desired in the Run Mode. Up to 102 characters can be stored in multiprogram sequence blocks. Each block, or program, can be executed individually or the operator can make the decision to branch to specific programs, run each in series or perform intermediate calculations from the keyboard. When programming in the Load Mode, the Delete key provides a convenient editing feature and the Halt key programs variable data entry points where control is temporarily returned to the operator in the Run Mode. Start and Skip keys control operation in both modes.

Synchronization with the calculator chip is accomplished by monitoring its Digit Output and Ready signals. The digit signals give timing information while the Ready indicates status of the calculator and synchronizes the key entry interface between it and the MM5766. Up to four switch inputs (K1, K2, K3 and K4) and up to twelve digit lines are connected in parallel with the calculator switch and digit terminals that scan the keyboard. Keys stored in the MM5766 that are entered by selecting K1 through K4 are encoded simply as matrix positions, i.e., a particular switch input at a specific digit time. Therefore it is the key matrix address that is stored and not the key function. Please refer to the MM5765 data sheet for a detailed functional description.

features

- Any key sequence, including constants and data entry points, may be stored automatically in the Load Mode and executed in the Run Mode.
- 102 step storage capacity of up to 47 different keys arranged in a 12 x 4 matrix.
- Multiprogram capability
- Provision for editing in Load Mode using the Delete key
- Convenient verification of programs using a Step Mode feature
- Alarm for full storage condition—or if a deletion of the first step in a program is attempted
- Power-on clear

block and connection diagrams Dual-In-Line Package 612-BIT STORAGE REGISTER CONTROL WORD I/O REGISTER COMMUTATOR READY ENCOGERA RUN/LOAD MAIN TEST ALARM DIGIT D11 I/O TIMING POWER ON SWITCH D3 AND 1/0 CONTROL D2 LOAD/RUN MODE 12 TOP VIEW Order Number MM5766N KEY DEBOUNCE K5. CONTROL INPUT See Package 21 FIGURE 1

 $\begin{array}{c} \textbf{absolute maximum ratings} \\ \textbf{Voltage at Any Pin Relative to V}_{SS} & \textbf{V}_{SS} + \textbf{0.3V to V}_{SS} - \textbf{12V} \\ \textbf{(All other pins connected to V}_{SS}) \end{array}$

Ambient Operating Temperature

0°C to +70°C Ambient Storage Temperature -55°C to +150°C 300°C Lead Temperature (Soldering, 10 seconds)

operating voltage range V_{SS} -6.5V \leq V_{DD} \leq V_{SS} -9.5V

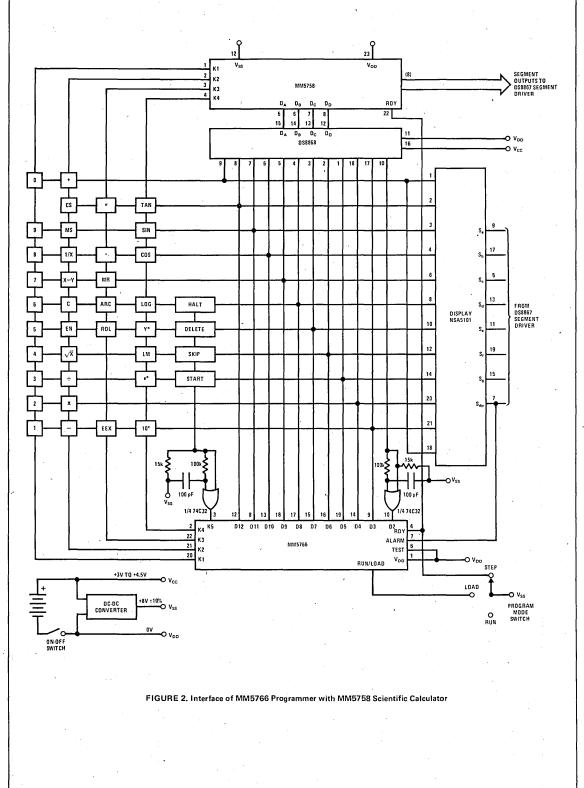
(V_{SS} is always the most positive supply)

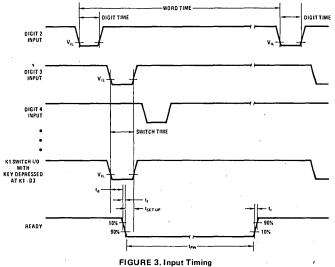
dc electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
1 _{DD}	. Operating Supply Current	$V_{DD} = V_{SS} - 9.5V, T_A = 25^{\circ}C$		8.0	18.0	mA
	Keyboard Scan Input Levels		ı			
	(K1, K2, K3, K4)			Ì		
V _{IH}	Logical High Level	$V_{DD} \approx V_{SS} - 7.2V$	V _{SS} -2.5	1	1 :	V
		$V_{DD} = V_{SS} - 8.8V$	V _{SS} -4.0			V
VIL	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			V _{DD} +1.0	V
		V _{DD} = V _{SS} - 9.5V	1	l	V _{DD} +1.5	V
	K5 and Digit Input Levels	•	ľ			
	(D2 through D12)			٠	1.	
V _{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.2V; I_{IH} \ge -200\mu A$	V _{SS} -2.5			V
		$V_{DD} = V_{SS} - 8.8V$; $I_{IH} \ge -200\mu A$	V _{SS} -4.0		1 1	· V
VIL	Logical Low Level	V _{DD} ¬ V _{SS} ~ 6.5V			V _{DD} +1.0	V
		$V_{DD} = V_{SS} - 9.5V$			V _{DD} +1.5	V
	Other Inputs (Ready, Run and Test)	1	. 1	١.		
VIH	Logical High Level		V _{SS} -2.5			· v
VIL	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			V _{SS} -5.0	V
		V _{DD} = V _{SS} - 9.5V			V _{SS} -6.0	· v
	Switch Buffer Output Levels					
	(K1, K2, K3, K4)		1	١	1 1	
V _{OH}	Logical High Level	$V_{DD} = V_{SS} - 7.2V$	V _{SS} -1.5		· V _{SS}	V
		$V_{DD} = V_{SS} - 8.8V$	V _{SS} -3.0		V _{SS}	V
V _{OL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			V _{SS} -6.0	V
		$V_{DD} = V_{SS} - 9.5V$, $I_{OL} \le -1.5 \text{mA}$			V _{SS} -7.0	V
	Alarm Output Current		1	· .		
	Source Current	$V_{OUT} = V_{SS} - 4.5V, V_{DD} = V_{SS} - 6.5V$	-5.0			mA
		$V_{OUT} = V_{SS} - 5.2V, V_{DD} = V_{SS} - 7.25V$	1	-8.0		mA
		$V_{OUT} = V_{SS} - 7.8V, V_{DD} = V_{SS} - 9.5V$			-20.0	mA

ac electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Digit Input Time	(Figure 3)	70			μs
	Word Time	(Figure 3)	0.64			ms
	Switch Input Time	(Figure 3)	70		ļ	μs
	Switch Output Time	(Figure 4)	70			μς
	Switch Propagation Delay Output	(Figure 4)		15	26	μs
t_R and t_F	Switch Output Transition Time	C _{LOAD} = 100 pF, (Figure 4)		2		μs
	Switch Input K5 Key Bounce out Stability Time (The time a keyboard input must be		4.5		17.0	ms
	continuously higher than the minimum Logical High Level to be accepted as a					5.
;	key closure, or lower than the maximum Logical Low Level to be accepted as a key release, i.e., 6 or 7 cycles of D2.)		V			
	Ready Timing	(Figure 3)	j			
t _R =t _F				3	5	·μs
t _D t _{SET:UP} t _{PW}			0.1 20 400	,	,	μs μs μs
	Key Closure Rate (Time between consecutive key outputs in Run Mode.)			40		ms
	Key Acceptance Rate (Time between consecutive key inputs in Load Mode.)				47	ms





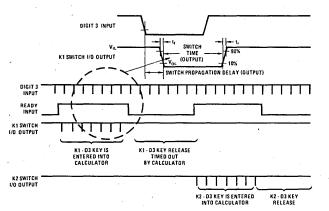


FIGURE 4. Programmer Output Timing