USING STANDARD NATIONAL CALCULATORS IN INDUSTRIAL AND MICROPROCESSOR APPLICATIONS

It is frequently desirable to utilize a calculator component in non-calculator applications. Because of their low cost, these devices represent a cost effective method of sophisticated number processing. A few hints that are worthwhile to keep in mind when applying calculators are listed below.

KEYBOUNCE AND NOISE REJECTION

The National line of calculators are designed to interface with low-cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

When a key closure is sensed by the calculator, an internal time-out is started. Any voltage perturbations of significant magnitude which occur on the Key Input Lines during the time-out will reset the timer to zero. A key is accepted as valid only after a noise-free time-out period: noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state, the output is at a logical high level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is complete and the key entry is accepted as valid. As the calculator begins to process the key, Ready goes low (near V_{DD}).

Ready remains at a low level until the function initiated by the key is complete *and* the key is released and timed out. The low-to-high transition indicates the calculator has returned to the "idle" state and a new key can be entered. *Figure 1* shows the relationship between keyboard entries and Ready.

Ready can be very helpful in a non-calculator application. It can be used in the following manner:

1) Whenever Ready is at a logic high, enter keys.
2) Whenever Ready is at a logic low, inhibit all keys and wait.
3) The transition from low to high indicates that an external machine can change states. Also, after a period of time, the display is valid and can be sampled.

ZERO SUPPRESSION

All calculators have some form of zero suppression. For left-justified displays, it is trailing zero suppression which is relatively easy to implement and fast. Right-justified displays require leading zero suppression. While this doesn't require much more logic, it is much slower. This can play an important role in using a calculator which must transfer results to other logic elements. After Ready goes high, it can take up to 7 word times before the segment information is correct. Consult Table I for specifics.

Figure 2 illustrates circuits for accomplishing the speed-ups given in Table I.

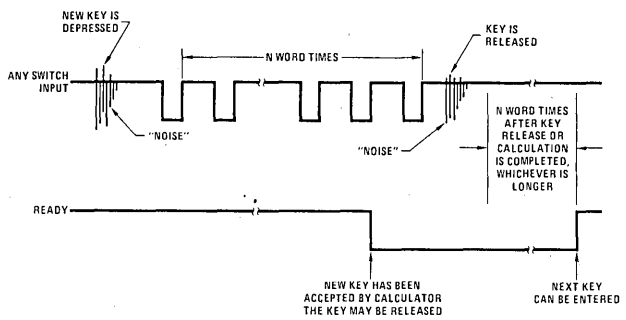
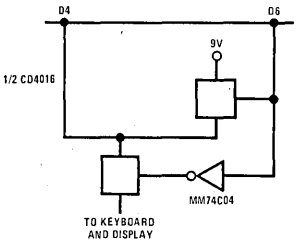


FIGURE 1. Functional Description of Ready Signal and Key Entry



If the inverter is unavailable, a CD4016 and resistor suffice.

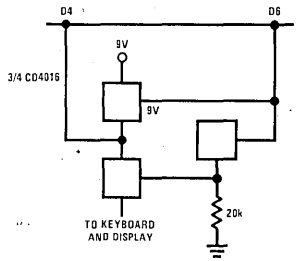


FIGURE 2. Calculator Speed Up Circuits

In many cases, a calculator circuit can be applied in a microprocessor system to eliminate the necessity of writing extensive floating point software routines. *Figure 3* shows such a system developed for a SC/MP microprocessor. Due to variations in power supply voltages and logic levels between SC/MP and the MM5760 Mathematician calculator, a combination of CMOS and low power Schottky components has been used. The MM5760 was chosen for this particular application because 3 other pin compatible calculators, the MM5762, MM5763 and MM5764 (Statistical, Financial and Metric Conversion) calculators will fit into the same socket and provide different algorithms.

Table II describes these functions and the codes that the SC/MP must present to the input register. SC/MP may operate either in an interrupt driven mode or through the use of the sense input. When programming the SC/MP calculator systems, it is advisable to perform the functions in the same manner as one would when operating the corresponding Novus or National Semiconductor calculator.

TABLE I

CALCULATOR	NORMAL KEY BOUNCE TIME	DEFEATED KEY BOUNCE TIME	HOW TO DEFEAT KEYBOUNCE	READY	DISPLAY CORRECT FOLLOWING READY PLUS	POWER ON CLEAR	LONG CAL	WHEN CAN SEGMENTS BE SAMPLED
MM5736, MM5749 MM5757	7–8 words	3-4 words	D4 high during D6	No		No	220 ms	Middle of digits
MM5737	7–8 words	3–4 words	D7 high during D9	Yes	7 words	No	350 ms	Trailing edge of digits
MM5738	7–8 words	3–4 words	D7 high during D9	Yes	7 words	No	350 ms	Trailing edge of digits
MM5739	7–8 words	3–4 words	D4 high during D9	No		No	300 ms	Middle of digits
MM5756	7 words	4 words	TC high during D3	Yes	0 words	Yes	3.1 sec	Middle of digits
MM5760, MM5762, MM5763, MM5764	9 words down, 16 words up	same	none	Yes	0 words	Yes	3 sec	Middle of digits
MM5765	Uses ready					Yes	40 ms	
MM5766	Uses ready					Yes	40 ms	
MM5780	7–8 words	3–4 words	D7 high during D9	Yes	0 words	No	350 ms	
MM5784	7–8 words	3–4 words	Connect K2 to D9	Yes	7 words	Yes	580 ms	Middle of digits
MM5791	11 words	2 words	Connect K2 to D9	Yes	7 words	Yes	580 ms	Middle of digits
MM5777	7–8 words	3–4 words	D6 high during D7	Yes	5 words	No	300 ms	Trailing edge of digits

TABLE II

CONTROL BYTE (HEXIDECIMAL)	FUNCTION OUTPUT SELECT FOR DIGITS 1–9			
00–08	MM5760	MM5762	MM5763	MM5764
11	–*	–	–	–
12	+*	+	+	+
13	÷*			
14	X*	X	X	X
15	–		Freq*	KS*
16	TAN	JAL*	$\overline{X}$	Ft–in
17	SIN	LOAN*	COR	In–mm
18	COS	SAV*	INT	IN–cm
20	1/X	SOD	Ex	mile-km
21	e^x	i*	REMy	Ft–m
22	y^x	AMT	y	–
23	LOG	–	X	MC
24	Ln	$Y^{\overline{X}}$	REMx	yd–m
25	Vx*	M+	M+	M+*
26	STO*	MR*	MR*	MR*
27	C	C	C	C
41	EN	=	=	=*
42	RCL	=+	=+	=+
43	k	CS	CS	CS*
44	•	•	•	•*
45	9	9	9	9*
46	8	8	8	8*
47	7	7	7	7*
48	6	6	6	6*
80	5	5	5	5*
81	4	4	4	4*
82	3	3	3	3*
83	2	2	2	2*
84	1	1	1	1*
85	0	0	0	0*
86	ARC*	n*	CA*	–
87	CS	%	%	%*

*Multiple function key–refer to individual data sheets

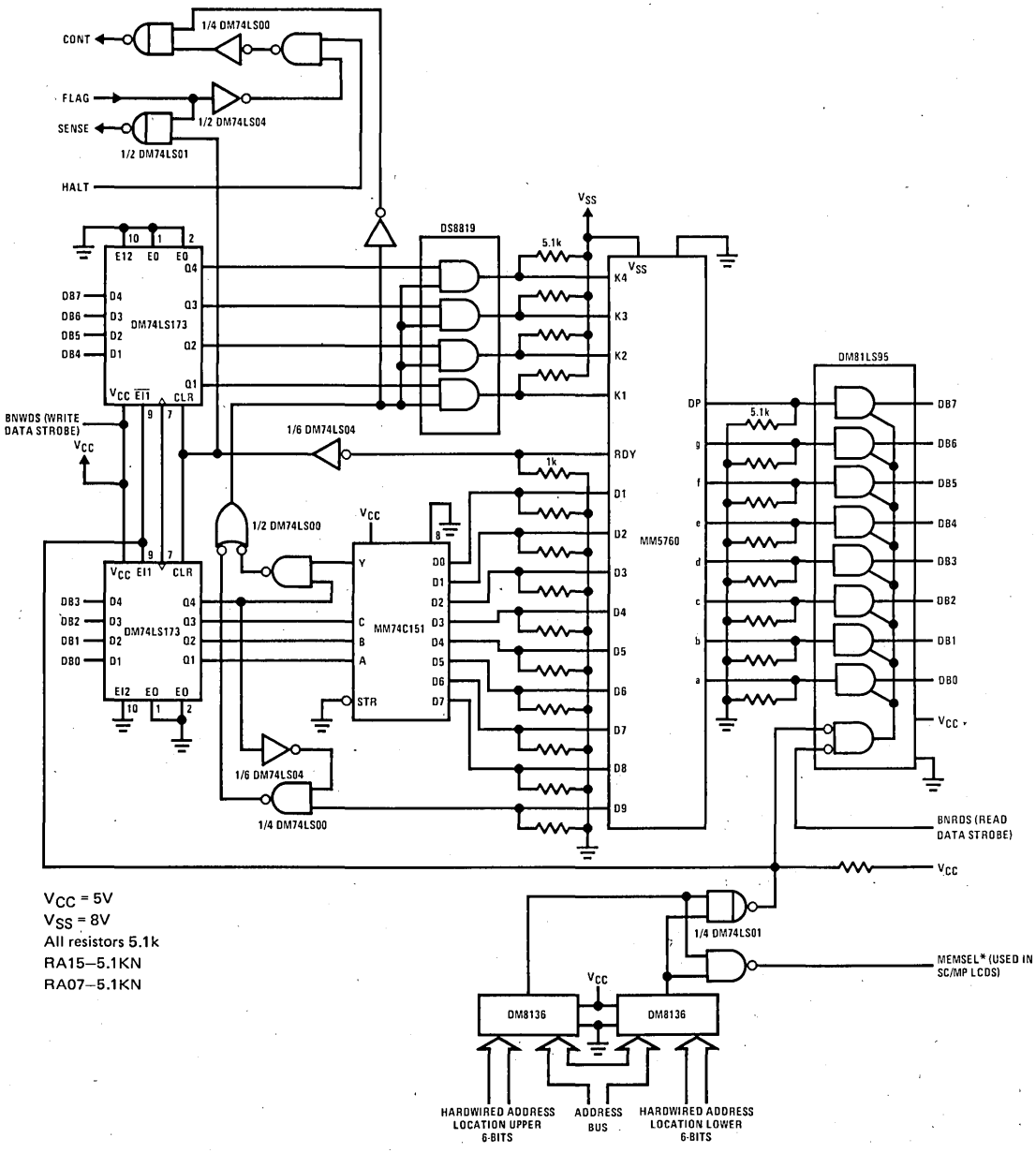


FIGURE 3. MM5760 SC/MP Interface

Operation of the circuit is straight forward; when the 8-bit control word is applied to the input register, a 9-bit multiplexer is addressed by the lower 4 bits, selecting a digit line. The upper 4 bits then gate the digit output through to the key inputs; the Ready line clears the input register and indicates acceptance to the processor. When the Ready line returns to its original state, another command may be entered. To receive the output of the calculator, the processor should load the lower 4 digits of the input register with the code corresponding to the digits required and the upper 4 digits with zeroes—the multiplexer output signal then indicates availability of data.

In an SC/MP system, synchronization with data is accomplished by first loading the digit code as described and

immediately entering the HALT state. The multiplexer output then drives the CONTINUE input. On start-up, the processor immediately loads the data.

In the application shown, 7-segment data plus decimal point is output to the data bus. Alternatively, one can use a 7-segment to BCD converter, DM86L25 or MM74C915, to connect the calculator output to BCD data.

A sample flow chart for the microcomputer program is depicted in *Figure 4*.

In summary, a reasonably low cost, low speed, arithmetic capability may be added to most systems using existing calculator components and standard logic.

TABLE III. Hexidecimal Conversion for 7-Segment Output

DIGIT	WITHOUT DECIMAL POINT	WITH DECIMAL POINT
0	3F	BF
1	06	86
2	5B	DB
3	4F	CF
4	66	E6
5	6D	ED
6	7D	FD
7	07	87
8	7F	FF
9	6F	EF
·		80
BLANK	00	80

Note: 0.0.0.0.0.0.0.0. indicates an illegal entry. All decimal points indicate the battery save mode.

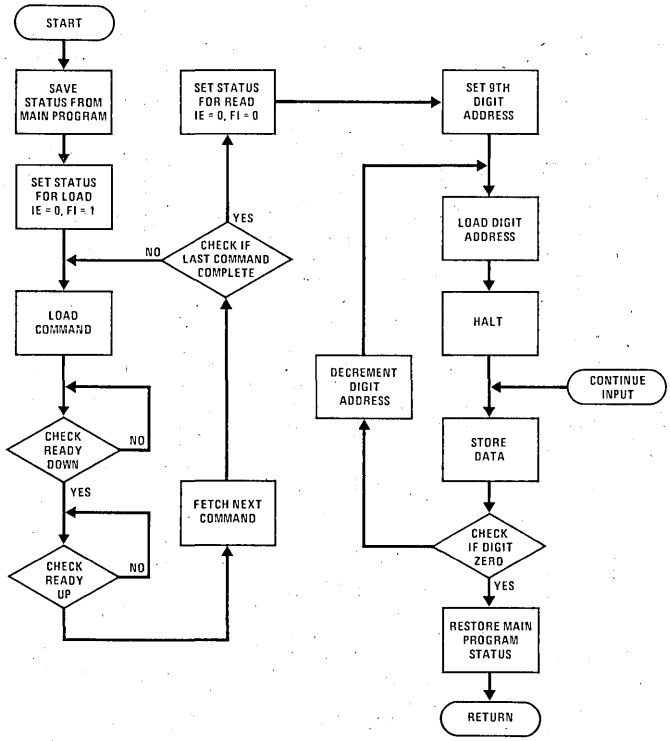


FIGURE 4