MM57109 MOS/LSI Number-Oriented Microprocessor

General Description

The MM57109 is an MOS/LSI number-oriented microprocessor intended for use in number processing applications. Scientific calculator functions, test and branch capability, internal number storage, and input/ output instructions have been combined in this single chip device. Programming is done in calculator keyboard level language with software development simplified and generated code more reliable because algorithms are preprogrammed in an on-chip ROM. Data or instructions can be synchronous or asynchronous; I/O digit count, I/O notation mode, and error control are user programmable; a sense input and flag outputs are available for single bit control.

The MM57109 can be used as a stand-alone processor with external ROM/PROM and program counter (PC). Alternatively it can be configured as a peripheral device on the bus of a microprocessor or minicomputer.

Applications

Instruments

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- Microprocessor/minicomputer extension
- Test equipment
- Process controllers

Features

- Scientific calculator instructions (RPN)
 - Up to 8-digit mantissa, 2-digit exponent
 - · Four-register stack, one memory register
 - Trigonometric functions, logarithmic functions, Y^X, e^X, π, etc.
 Error flag generation and recovery
 - Entor hag generation
- Flexible input/output
 HOLD input allows asynchronous instructions or
 - single stepping Asynchronous digit input instruction (AIN) with
 - AIN ready (ADR) input Multidigit I/O instructions (IN, OUT) with floating
 - point or scientific notations
 Programmable mantissa digit count for IN, OUT instructions
 - Sense input and flag outputs
- Branch control
 - Conditional and unconditional program branching
 Increment/decrement branch on non-zero for program loops
- Interface simplicity
 - Single ϕ clock
 - Low power operation
 - Generation of I/O control signals
 - Separate digit input, output, and address bus

TABLE I. Feature Comparison of LSI Number Processing Chips

FUNCTION	CALCULATOR	MM57109	MICRO- PROCESSOR
1/0	Keyboard display	Multidigit asynchronous cigit single bit	Deta bytes / single bit
Data format	Floating point Scientific Notation	Floating point Scientific Notation	Binary
Data length	Fixed	Variable (1 to 8 digit mantissa)	Fixed
Program	Key sequence	External ROM/ PC, μP or FIFO	External ROM Internal PC
Speed (math or I/O operations)	14–400 ms	0.5-400 ms	0.5500 ms
Minimum number of thips for CPU and RAM	1–3	1 (external PC and program sou rc e)	2–6

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Absolute Maximum Ratings

 $\label{eq:Voltage at Any Pin Relative to V_{SS}} V_{SS} + 0.3V \ to \ V_{SS} - 12V \\ (All Other Pins Connected to V_{SS}) \\ Ambient Operating Temperature 0° C to +70° C \\ \end{array}$

Ambient Storage Temperature Lead Temperature (Soldering, 10 seconds)

-55°C to +125°C 300°C

> tpdDAS trDAS DA1-DA4, BR (tpdg D01-D04, F1 Timing tpdK Connectior

> > 11/01 -1 12/02 -7 13/03 -3 14/04 -4 14/04 -4 19/ADA -5 SYNC -5 SSNC -5 SSNC

Switching

OSC (INPUT)

SYNC (OUTPUT)

R/W, ISEL (OUTPUTS)

DAS (OUTPUT)

DA1-DA4, BR (OUTPUTS) VO

001-004, F1, F2, RDY, ERROR (OUTPUTS)

VIL INT

Vol

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DC Electrical Characteristics ($0^{\circ}C \le T_A \le +70^{\circ}C$, 7.9V $\le V_{SS} - V_{DD} \le 9.5V$ unless otherwise stated)

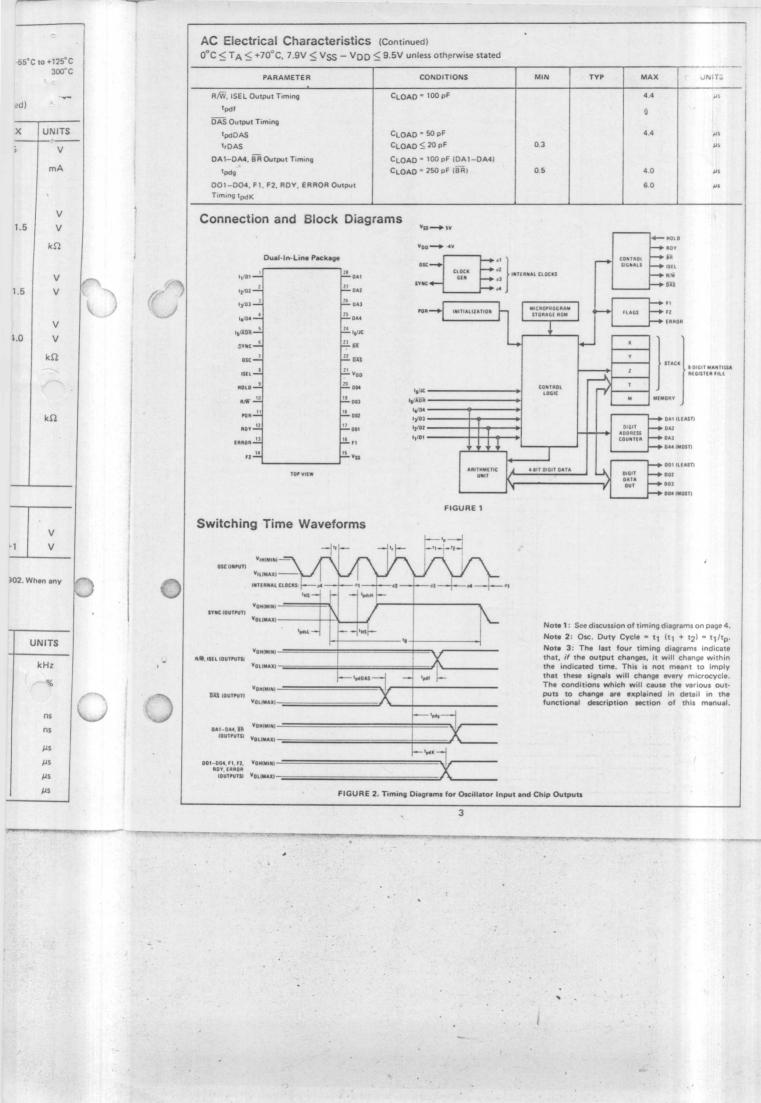
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage (VSS - VDD)		7.9		9.5	V
Operating Supply Current (IDD)	V _{SS} - V _{DD} = 9.5V, T _A = 25°C (Excluding Outputs)		12	18	mA
Osc. Input Voltage Levels					
Logic High Level (VIH)	$V_{SS} - V_{DD} = 7.9V$	V _{SS} -1.0			V
Logic Low Level (VIL)	$V_{SS} - V_{DD} = 9.5V$		•	VDD+1.5	V
Osc. Input Resistance to VSS			6		kΩ
HOLD, POR Input Voltage Levels					
Logic High Level (VIH)		VSS-3.0			V
Logic Low Level (VIL)				VDD+1.5	V
11-16 Input Voltage Levels	(Note 1)				
Input High Level (VIH)		V _{SS} -1.0			V
Input Low Level (VIL)				VSS-4.0	V
R/W, Sync, ISEL, BR		9.1			kΩ
External Load Resistor to VDD	$V_{OH} \ge V_{SS} - 2.3V$,	(Can Drive			
to Drive TTL	(Note 2)	1 LPTTL			
		Load)			
DO1-DO4, F1, F2, Error and Ready	$V_{OH} \ge V_{SS} - 2.3V$,	2			kΩ
External Load Resistor to VDD	(Note 2)	(Drives			
to Drive TTL		1 TTL or			
		5 LPTTL			
		Loads)		1.1.1.1	

All Outputs	External Resistor to GND =			
Output High Voltage (VOH)	10 kΩ	V _{SS} -1	VSS	V
Output Low Voltage (VOL) $^{\circ}$		VDD	V _{DD} +1	V

Note 1: An external resistor from 5k to 20 k Ω must be tied at the I₆ input to V_{SS} to overcome internal load device to V_{DD}. Note 2: Outputs DA1–DA4 and DAS cannot drive LPTTL directly and must be buffered by a CMOS driver such as the MM54C902. When any output drives CMOS an external load resistor of 10 k Ω to 20 k Ω must be provided to CMOS ground.

AC Electrical Characteristics $0^{\circ}C \le T_A \le +70^{\circ}C$, 7.9V $\le V_{SS} - V_{DD} \le 9.5V$ unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Osc. Input Frequency		320		400	kHz
Osc. Duty Cycle	(Figure 2)	46	56	66	%
Osc. Input Rise Time (t _r) Fall Time (t _f)	CLOAD = 25 pF, RLOAD = 6 kΩ RC = 0.15 μs			350 50	ns ns
SYNC Output Interval tB (1 microcycle)	CLOAD = 250 pF	10.0		12.5	μs
^t pds L		0.1		1.65	μs
tpdsH		0.1		1.25	μs
tHS		0.1		0.8	μs



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Timing Diagram Conventions

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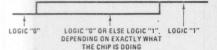
world.

This data sheet makes extensive use of timing diagrams to illustrate electrical and logical characteristics of signal inputs and outputs. To avoid confusion concerning these diagrams, the following conventions have been adopted:

- 1. Time axis is horizontal, increasing to the right.
- 2. Upper side of waveform represents logic "1" (VSS). Lower side of waveform represents logic "0" (VDD).



03. Lines appearing simultaneously at both logic "O" and logic "1" indicate that the state of the input or output is either "O" or "1", and does not change during this time. This is used when the logic state depends on exactly what the user is doing with the chip at the time, and thus is unknown to the person drawing the timing waveform.



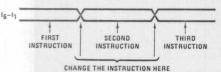
4. Lines located at a level between logic "1" and logic "O" appear on input signals only, and indicate that the state of the input is a don't care during this time.



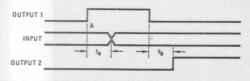
5. An "X" in a waveform indicates that the input or output may change state at this time.



This representation is often used for a group of inputs or outputs whose logic states are unknown, but the time at which a signal may change must be shown. Example:



6. Minimum and/or maximum time values are sometimes specified. The interpretation of these values depends on whether the waveforms are inputs or outputs. Example:



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The following table shows three different ways in which these timing diagrams can be interpreted:

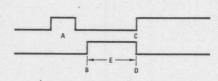
PARA	METER	MIN	MAX	COMMENT
(A)	ta	3.7 μs		Input must be changed later than 3.7 μ s after point "A"
	tb		1.9 ms	Output 2 will go high no later than 1.9 ms after output 1 goes low
В)	ta		2.4 ns	Input must be changed before 2.4 ns after point "A"
	tb	0.7 s		Output 2 will not go high until at least 0.7 s after output 1 goes low
C)	ta	0.6 μs	3.0 μs	Input must be changed between 0.6 and 3.0 μ s after point "A", no sooner and no later
	tb	0.01 μs	0.9 µs	Output 2 will go high between 0.01 and 0.9 μ s after output 1 goes

This illustrates the various meanings that must be attached to time values, depending on whether they refer to inputs or outputs and whether minimum, maximum or min/max limits are placed on the value.

low

7. Rise and fall times are measured from maximum logic low to minimum logic high. For example, if the maximum logic low ("0") level ($V_L(MAX)$) of a signal is VDD + 1V, and if the minimum logic high ("1") level $(V_{H(MIN)})$ is $V_{SS} - 1.5V$, then the rise time would be the time it takes the signal to go from VDD + 1V to VSS - 1.5V.

Timing diagrams are seldom shown to scale because of space limitations. However, they do show the proper relationship between waveforms. Consequently, the reader, len studying a timing diagram, should exercise care in understanding what information the timing diagram is meant to show, and ignore the time scale distortions that are necessarily introduced. Example:



Waveform relationships are maintained, so pulse A does come before B, and C and D occur at the same time. However, the time axis may be distorted, so pulse width E may not be twice that of pulse A. It may be 10 times, or even 1000 times wider.

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The processor and then setti patible.) The their proper These ready p processing of a titled Error ignore the firs "Ready for In

of instruction

Functional Description

The MM57109 is intended for microprocessor number processing applications, either as a microprocessor peripheral chip or as a stand-alone processor. Figure 1 shows a pinout diagram of the MM57109, giving the pin numbers and names of the signal lines. It also shows a functional block diagram illustrating the internal organization of the MM57109 and the origin of these signal lines that are used to communicate with the external world.

The MM57109 operates on a 9V power supply. In order to make it TTL compatible, it can be operated from supplies of 5V and -4V. The signal inputs are designed to respond properly to TTL logic levels (with the exception of HOLD and POR) when the MM57109 is operated in this fashion. (See electrical specifications and Figure 3 for details on LPTTL interface).

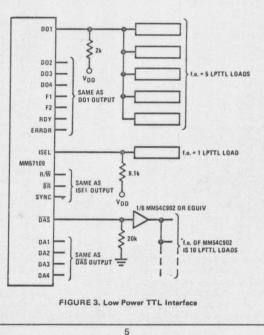
A 400 kHz oscillator operating between 0V and 5V is required. The rise and fall times and frequency of this oscillator are not critical, making it relatively easy to generate. The MM57109 provides a SYNC output, which is a signal that goes active low once every 4 oscillator cycles. A single SYNC pulse corresponds to a single "microcycle" (about 10 μs). The execution of a single MM57109 instruction involves thousands of microcycles. A later section of this manual will contain a tabulation of instruction execution times listed in microcycles.

The processor is reset by applying 5V to the POR pin and then setting it to -4V. (This input is not TTL compatible.) The chip will then set the various outputs to their proper levels and generate 3 ready pulses (RDY). These ready pulses are designed to provide for automatic processing of an error in stand-alone systems. (See section titled Error Control.) A microprocessor system would ignore the first 2 RDY pulses and use the third one as a "Ready for Instruction" signal.

The MM57109 has 6 instruction inputs (I6-I1) which are used to provide it with a 6-bit instruction code (commonly referred to as an "op code"). This op code corresponds to one of the MM57109 instructions. A list of instructions, their op codes, and a description of what they do will be given later in this manual. The 6 instruction lines are shared by 6 data lines. The output ISEL identifies which function the 6 lines are performing. When ISEL = 1, the 6 lines are instruction lines (I_6-I_1) . When ISEL = 0, the 6 lines are data lines (JC, ADR, D4-D1). In many cases the data lines, which are associated with the IN, AIN, and TJC instructions, will not be used. In these instances ISEL can be ignored. If the data lines are used, ISEL is the select input for six 2-1 multiplexers or an enable input to buffers, latches or ROMs. Later in this manual sample systems will be shown illustrating use of ISEL.

A ready output (RDY) goes high when the processor is ready to read a 6-bit instruction code. This output operates in conjunction with the HOLD input. When RDY goes high, it will remain high if HOLD = 1. If processor instructions are not always ready when RDY goes high, some method must be provided to set HOLD 1. A microprocessor might have a flag output which holds HOLD = 1 until it is ready to pass an instruction to the processor. (If instructions are always ready when RDY goes high, the HOLD input can be tied to "0".) After RDY goes high, it will wait for HOLD = 0 and then go low again. At this time the 6-bit instruction code is read and the instruction is performed.

The branch output (BR) is a 4-microcycle active low pulse which signals that the result of a test instruction (e.g. TEST X = 0) was true. This pulse starts prior to RDY = 1 for the next instruction, and ends slightly after RDY = 1.



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The 3 signals RDY, HOLD, and ISEL were carefully chosen to allow the MM57109 to be used as a stand-alone processor or as a microprocessor peripheral. In a standalone system, RDY would be a clock for an external program counter (PC) whose outputs would address a ROM containing the MM57109 instructions. BR would parallel load the PC, resulting in a program branch. In a microprocessor system, RDY would inform the microprocessor that the processor is ready for a new instruction. HOLD would be used to give the microprocessor time to respond to the MM57109.

As shown in Figure 1, the chip has an internal register file. Each of the 5 registers (X, Y, Z, T, and M) has 8 mantissa digits, 2 exponent digits, a decimal point position indicator, and mantissa and exponent sign bits. Instructions operate on these registers. The instructions IN and OUT input and output numbers to and from the X register. There are 2 possible modes of operation for IN and OUT instructions. Floating point mode transfers mantissa digits, a mantissa sign digit, and a decimal point position digit. Scientific notation mode transfers mantissa digits, 2 exponent digits, a digit containing mantissa and exponent sign bits, and a decimal point position indicator. Initially the MM57109 is in the floating point mode. The TOGM instruction toggles to the opposite mode. The number of mantissa digits input or output by an IN or OUT instruction is equal to the mantissa digit count (MDC). The MDC is initially 8 and can be set to any value from 1 to 8 using the SMDC instruction. When an IN or OUT instruction is executed, the four DA outputs will sequence through values indicating which digit is to be input or output. The section of this manual entitled Data Formats shows the values of the DA lines for each of the digits input or output by an IN or OUT instruction. During an OUT instruction, the four DO outputs provide the digit outputs, coded in BCD. The R/W output is pulsed active low once for each digit. This R/W pulse can be used to write the data into a RAM or clock it into a latch. During an IN instruction, the four I lines (I4-I1), are data input lines for the digits to be input and so are also named D4-D1. The same data format is used for IN as is used for OUT. The DAS output is pulsed active low prior to reading each digit. This DAS pulse can be used as a data request signal to clock data into a latch. The digit address on the DA lines is valid on the positive-going edge of the DAS pulse.

The IN and OUT instructions have been designed to allow easy expansion of the internal register file. A 256 x 4 RAM will add an additional 16 registers for data storage. The DA lines are used to provide part of the RAM address. The rest of the address, which would specify one of the 16 registers, comes from the external instruction storage (ROM, microprocessor, etc). The DO lines are the input to the RAM, while the RAM outputs are multiplexed to the I lines, using ISEL to select between instructions or data. The processor R/W line is the RAM R/W signal.

There are three ways to input data to the MM57109. The first is the IN instruction which has already been described. Second is the AIN instruction, which inputs a single digit into the X register. Multiple AIN instructions will input more than one digit to the X register, since the AIN instruction does not cause termination of

the number entry mode (number entry mode will be fully described later in this manual). The DA lines provide a digit address from 0 to 7 for multiple AIN instructions. The $\overline{\text{ADR}}$ input (shared with 1₆) is a data hold signal for AIN. If $\overline{\text{ADR}}$ is high during an AIN instruction, the processor will wait till it goes low, and then read the digit on D4-D1. Finally, the F2 output of the MM57109 will be pulsed active low as a read acknowledge signal.

For systems using a microprocessor with the MM57109 as a peripheral, it is unlikely that the IN nor the AIN instruction would be used. Instead, the third method of inputting data to the processor would be used. This method involves entering numbers as instructions. There are "0", "1", "2", ... "9" instructions, a decimal point instruction, etc. A number can be entered directly into the processor in the same manner as one presses keys to enter numbers into a calculator.

Several instructions have conditions which will cause an error to occur. Table III will enumerate these conditions. When an error does occur, the MM57109 will set the ERROR output high. This output can be tested with the TERR instruction and cleared with the ECLR instruction.

The 2 outputs F1 and F2 are flags which are set by the instructions SF1 and SF2. They can also be pulsed active high with the instructions PF1 and PF2. These flag outputs could be used as single bit outputs from the MM57109.

A TJC instruction will branch (i.e. result in a true condition causing a \overline{BR} pulse) if the input JC is high. Otherwise the TJC instruction will do nothing.

Table II summarizes this description of the MM57109 signal lines.

2-WORD INSTRUCTIONS

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Several instructions are 2-word instructions, of which there are 4 types. Each type generates 2 RDY pulses, one for each word. The first type are the inverse instructions (inverse SIN, COS, TAN and inverse +, -, x, ÷ for memory operations). These instructions require that the INV instruction first be executed, followed by the desired instruction (SIN, COS, etc.). The second type is the SMDC instruction. The second word of this instruction is the mantissa digit count, a BCD number from 1 to 8. The third type is the IN and OUT instructions. The second word of these instructions is the register number (i.e. the high order address for a RAM) or possibly a device select code. It is not necessary to use the second word of these instructions because the MM57109 ignores it, providing only a RDY pulse that may or may not be used by external hardware. The final type of 2-word instructions are the branch instructions. The second word of these instructions is intended to be a branch address to be loaded into an external program counter in stand-alone systems. For a microprocessor system, the second RDY pulse can be used to clock the BR output into a latch. The latch can then be tested to discover if the branch condition was true (BR = 0) or false (BR = 1). Many microprocessor applications will not use the branch instructions, since testing and branching is often more easily done within the microprocessor itself.

Functional MNEMONIC VSS, VDD POR osc SYNC RDY HOLD BR ISEL R/W In. JC IS, ADR 14-11, D4-D1 DA4-DA1 DAS D04-D01 F1 F2 ERROR

mode will be DA lines pro-AIN instruca data hold N instruction, then read the the MM57109 wledge signal.

the MM57109 nor the AIN ird method of be used. This uctions. There cimal point I directly into presses keys to

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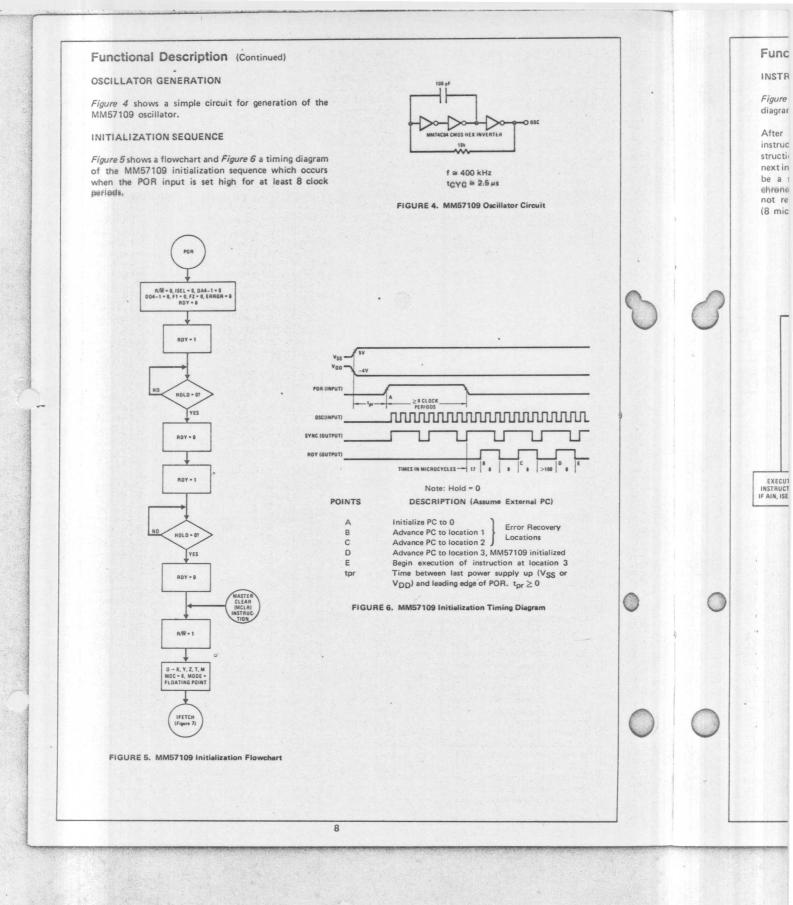
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ns, of which Y pulses, one a instructions \neg , x, \doteq for quire that the weed by the second type d of this in-BCD number OUT instructions is the b for a RAM) bessary to use because the Y pulse that are. The final instructions are. The final instructions to clock the b be tested to (BR = 0) or lications will testing and n the micro-

			1	TABLE II. MM57109 Pin Descri	ption
		MNEMONIC	PIN NUMBER	FUNCTIONAL NAME	DESCRIPTION
		V _{SS} , V _{DD}	15, 21	V _{SS} , V _{DD}	V _{SS} = V _{DD} + 9V nominally (see electrical specifica- tions) (V _{SS} = Logic ''1'')
		POR	11	Power ON Reset	Set high for at least 8 oscillator periods to power ON. MM57109 will then set R/W = 1, other outputs = 0, and generate 3 ready pulses before reading first instruction. HOLD must be 0 to complete each ready pulse.
		OSC	7	Oscillator Input	Single ϕ clock with frequency 4X microcycle time. Typical frequency is 400 kHz.
	4	SYNC	6	Sync Output	Active low output pulse once each microcycle.
		RDY	12	Ready	Rising edge indicates processor is ready to execute next instruction or get second word of 2-word in- struction. If HOLD = 0, RDY goes low again and nex instruction is executed. If HOLD = 1, RDY stays high until HOLD = 0. (See Figure 8). RDY can be used to clock an external program counter or to request an instruction from another CPU.
G	0	HOLD	9	Hold	When set high prior to or at the rising edge of RDY, RDY will be held high and instruction execution delayed until HOLD is set low.
		BR	23	Branch	A 4-microcycle active low pulse indicates a program branch. RDY goes high during this pulse. BR may be used as a load signal for an external PC or as a sense input to a microprocessor.
		ISEL	8	Instruction Select	Selects 6 bit instruction code (ISEL = 1) or JC, \overline{ADR} D4-D1 (ISEL = 0) on I ₆ -I ₁ (the 6 input lines)
		R/Ŵ	10	Read/Write	Active low pulses during OUT instruction to write data digits into a RAM or register. Address and data are valid at both edges. R/W is also pulsed during a PRW1 or PRW2 instruction.
		1 ₆ , JC	24	Input 6, Jump Condition	Most significant instruction bit when ISEL = 1. Jump condition for TJC instruction when ISEL = 0. (JC = 1 indicates jump condition true.)
		I5, ADR	5	Input 5, AIN Data Ready	Instruction bit 5 when ISEL = 1. AIN Data Ready (\overline{ADR}) for AIN instruction when ISEL = 0. \overline{ADR} = 0 for data ready.)
		I4-I1, D4-D1	4, 3, 2, 1	Inputs 4–1, Data 4–1	Instruction bits 4–1, or mantissa digit count on second word of SMDC instruction, when ISEL = 1. Digit data (AIN or IN instructions) when ISEL = 0. Bit 4 is the most significant bit.
	•	DA4DA1	25, 26, 27, 28	Digit Address 4–1	Digit address for AIN, IN, and OUT instructions Used as multiplex selector (AIN) or as low order ad dress (IN, OUT) for RAM or other I/O device. Bit 4 is the most significant bit. Blanked (=0) after each IN,OUT, or AIN instruction.
9		DAS	22	Digit Address Strobe	Active low pulse indicates digit address is changing New address is valid on second (positive-going) edge
		D04-D01	20, 19, 18, 17	Digit Outputs 4–1	BCD digit output for OUT instruction. Blanked (=0, after each OUT instruction. Bit 4 is the most signi ficant bit.
		F1.*	16	Flag 1	User controlled flag can be set or pulsed (reset if high).
0		F2	14	Flag 2	User controlled flag can be set or pulsed (reset if high). Active low pulse (set if low) generated after each AIN data read. This can be used as an acknowledge signal to clear a flip-flop.
0	0	ERROR	13	Error Flag	Set on an arithmetic or OUT error. Reset by ECLR instruction. See Error Control for more information.

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INSTRUCTION FETCH AND EXECUTION

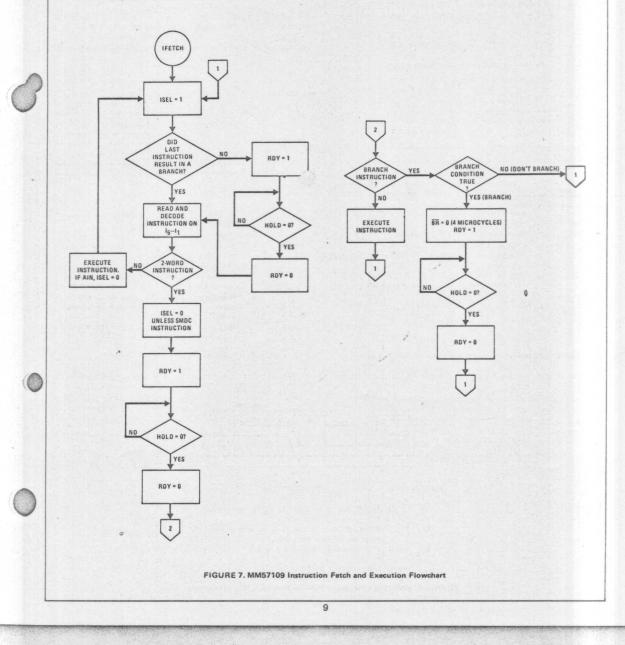
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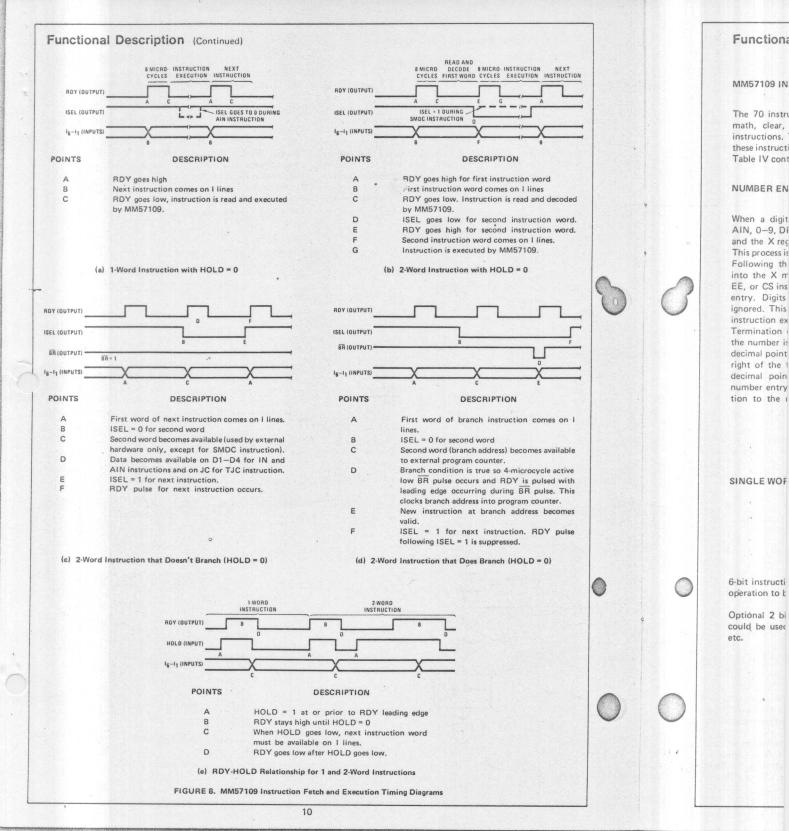
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Figure 7 shows a flowchart and Figure 8 shows a timing diagram of the instruction fetch and execution sequence.

After initialization (POR) or the completion of an instruction, the processor raises RDY to signal the instruction store device that the processor is ready for the next instruction word. The instruction store device could be a semiconductor memory, host CPU, or an asynchronous device of some kind. If the instruction store is not ready to respond within the required access time (8 microcycles), it must raise the HOLD input to delay the instruction word fetch. HOLD may be set high any time while RDY is low, or at the leading edge of RDY. When HOLD goes low the processor will lower RDY and begin instruction execution. The instruction word must remain valid while RDY is low. -

During program branches, skips, or fetching of the second word of a 2-word instruction, the RDY/HOLD sequence is the same as discussed above. (See flowchart in *Figure 7* and timing diagram in *Figure 8(e)*.)





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MM57109 INSTRUCTION SET

The 70 instructions are classed into digit entry, move, math, clear, branch, input/output, and mode control instructions. Table III contains a detailed description of these instructions. *Figure 9* shows the instruction format. Table IV contains a summary of the instructions.

NUMBER ENTRY

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When a digit, decimal point, or π is entered with an AIN, 0–9, DP, or PI instruction, the stack is first pushed and the X register cleared: $Z \rightarrow T$, $Y \rightarrow Z$, $X \rightarrow Y$, $O \rightarrow X$. This process is referred to as "initiation of number entry." Following this, the digit and future digits are entered into the X mantissa. Subsequent entry of digits or DP, EE, or CS instructions do not cause initiation of number entry. Digits following the eighth mantissa digit are ignored. This number entry mode is terminated by any instruction except 0-9, DP, EE, CS, PI, AIN or HALT. Termination of number entry means two things. First, the number is normalized by adjusting the exponent and decimal point position so that the decimal point is to the right of the first mantissa digit. Second, the next digit, decimal point, or π entered will cause initiation of number entry, as already described. There is one exception to the number entry initiation rule. The stack is

not pushed if the instruction prior to the entered digit was an ENTER. However, the X register is still cleared and the entered digit put in X.

The IN instruction enters *all* digits of a number. Therefore, IN does not cause initiation of number entry. However, it does terminate number entry mode if the processor is in this mode before the IN instruction is executed. This means the user can mix 0-9, AIN and IN instructions without performing an ENTER before an IN.

The IN instruction will always push the stack unless the previous instruction was ENTER. This allows multiple IN instructions to be executed without performing an ENTER between them.

INSTRUCTION TIMING

Table V shows execution times of each instruction. These times are shown in microcycles, 1 microcycle being equal to 1 SYNC period. *Figure 10* shows timing diagrams illustrating the dynamic characteristics of execution of each type of instruction, assuming HOLD = 0.

SINGLE WORD INSTRUCTIONS

2 1 16 15 14 13 12 11 EH OP CODE

6-bit instruction operation code (see Table III) specifies operation to be performed.

Optional 2 bits for external hardware (EH). These bits could be used for device selection on AIN instructions, etc.

2-WORD INSTRUCTIONS

2 1 16 15 14 13 12 11 EH OP CODE 8 7 6 5 4 3 2 1 Address or MDC

First word is the same format as 1-word instructions.

Second word contains branch address to be loaded into PC on branch, or MDC (Mantissa Digit Count) for SMDC instruction, or high order address bits for RAM on IN/OUT instructions. (Low order address from DA lines.) (Second word is ignored except for SMDC instruction. I lines must contain digit data during AIN, IN instructions.)

FIGURE 9. MM57109 Instruction Format

TABLE III. MM57109 Instruction Description Table (* Indicates 2-word instruction)

CLASS	SUBCLASS	MNEMONIC*	OCTAL OP CODE	FULL NAME	DESCRIPTION			CLAS
Digit Entry		0 1 .• 2 3 4	00 01 02 03 04	0 1 2 3 4 5	Mantissa or exponent digits. On first digit (d) the following occurs: $Z \rightarrow T$ $Y \rightarrow Z$ $X \rightarrow Y$ $d \rightarrow X$ See description of number entry on page 11.			Math
		5 6 7 8 9	05 06 07 10 11	6 7 8 9				
		DP EE CS	12 13 14	Decimal Point Enter Exponent Change Sign	Digits that follow will be mantissa fraction. Digits that follow will be exponent. Change sign of exponent or mantissa. Xm = X mantissa Xe = X exponent CS causes $-Xm \rightarrow Xm$ or $-Xe \rightarrow Xe$ depending	8	0	
		PI ° EN	15 41	Constant π Enter	on whether or not an EE instruction was executed after last number entry initiation. 3.1415927 \rightarrow X, stack not pushed. Terminates digit entry and pushes the stack. The argument entered will be in X and Y. $Z \rightarrow T$ $Y \rightarrow Z$ $X \rightarrow Y$			
		NOP	77	No Operation	Do nothing instruction that will terminate digit			•
		HALT	17	Halt	entry. External hardware detects HALT op code and generates HOLD = 1. Processor waits for HOLD = 0 before continuing. HALT acts as a NOP and may be inserted between digit entry instructions since it does not terminate digit entry.			
Move		ROLL	43	Roll	Roll Stack.			Clear
		POP	56	Рор	Pop Stack. $Y \rightarrow X$ $Z \rightarrow Y$ $T \rightarrow Z$ $O \rightarrow T$	•		Branc
		XEY	60	X exchange Y	Exchange X and Y. $X \leftrightarrow Y$			
		XEM	33	X exchange M	Exchange X with memory. $X \leftrightarrow M$			
	Q.	MS	34	Memory Store	Store X in Memory.	1		
	*	MR	35	Memory Recall	$X \rightarrow M$ Recall Memory into X.	1		
		LSH	36	Left Shift Xm	$M \rightarrow X$ X mantissa is left shifted while leaving decimal point in same position. Former most significant	0	0	
		RSH	37	Right Shift Xm	digit is saved in link digit. Least significant digit is zero. X mantissa is right shifted while leaving decimal point in same position. Link digit, which is			
					normally zero except after a left shift, is shifted into the most significant digit. Least significant digit is lost.			

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				TA	BLE III. MM57109	Instruction Desc	ion Table (Continued)	(* Indicates 2-word instruction)
4			CLASS	SUBCLASS	MNEMONIC*	OCTAL OP CODE	FULL NAME	. DESCRIPTION
git (d)			Math	F (X,Y)	+	71	Pluș	Add X to Y. X + Y \rightarrow X. On +, -, x, / and YX instructions, stack is popped as follows: $Z \rightarrow Y$ $T \rightarrow Z$ $O \rightarrow T$
ge 11.	T							Former X, Y are lost.
30	1	10000	1 States		-	72	Minus	Subtract X from Y. $Y - X \rightarrow X$
	· 1				x	73	Times	Multiply X times Y. $Y \times X \rightarrow X$
				and the second	1	74	Divide	Divide X into Y. $Y \div X \rightarrow X$
	1	1.2.2	10.355		YX	70	Y to X	Raise Y to X power. $Y^X \rightarrow X$
ction.				F (X,M)	INV +*	40, 71	Memory Plus	Add X to memory. $M + X \rightarrow M$ On INV +, -, x and / instructions, X, Y, Z and T are unchanged.
	6	0			INV-*	40, 72	Memory Minus	Subtract X from memory. $M - X \rightarrow M$
		65			INV x*	40, 73	Memory Times	Multiply X times memory. $M \times X \rightarrow M$
ending					INV /*	40, 74	Memory Divide	Divide X into memory. $M \div X \rightarrow M$
n was				F (X) Math	1/X	67	One Divided by X	$1 \div X \rightarrow X$. On all F (X) math instructions Y, Z
ation.		T. S. R. C.						T and M are unchanged and previous X is lost
	1				SORT	64	Square Root	$\sqrt{X} \rightarrow X$
stack.		*			SQ	63	Square	$X^2 \rightarrow X$
-					10X	62	Ten to X	$10^{X} \rightarrow X$ $e^{X} \rightarrow X$
					EX	61	E to X	
	1	Sec. Sec.			LN	65	Natural log of X	$ ln X \to X \\ log X \to X $
					LOG	66	Base 10 log of X Sine X	$SIN(X) \rightarrow X$. On all F(X) trig functions, Y, Z, T
e digit		N. S. S.	148 S.S.S.S.	F (X) Trig	SIN	44	Sine A	and M are unchanged and the previous X is lost
la and		1.22			cos	45	Cosine X	$COS(X) \rightarrow X$
le and HOLD		1		oʻ .	TAN	46	Tangent X	TAN(X) →X
Pand	1.1.1.1.1.1.1.1				INV SIN*	40, 44	Inverse sine X	$SIN^{-1}(X) \rightarrow X$
ctions					INV COS*	40, 45	Inverse cosine X	$\cos^{-1}(x) \rightarrow x$
			8-2-1-3-1-3-1-		INV TAN*	40, 46	Inverse tan X	$TAN^{-1}(X) \rightarrow X$
		1.155.931			DTR	55	Degrees to radians	Convert X from degrees to radians.
		2.482.584			RTD	54	Radians to degrees	Convert X from radians to degrees.
			Clear		MCLR	57	Master Clear	Clear all internal registers and memory; initializ I/O control signals, MDC = 8, MODE = floatin point. (See initialization.)
		A PAGE	The second		ECLR	53	Error flag clear	$O \rightarrow Error flag$
	0		Branch	Test	JMP*	25	Jump	Unconditional branch to address specified b second instruction word. On all branch instruc- tions, second word contains branch address t
	0	0			中心的感觉的		1.1.1.1.1.1.1.2.4.1	be loaded into external PC.
	9				TJC*	20	Test jump condition	Branch to address specified by second instruction word if JC (I ₆) is true (=1). Otherwise
	I I I I I I I I I I I I I I I I I I I				TERR*	» 24	Test error	skip over second word. Branch to address specified by second instruc- tion word if error flag is true (= 1). Otherwise
0	1							skip over second word. May be used for detecting specific errors as opposed to using the automatic error recovery scheme dealt with it
CI	0		12.142					the section on Error Control.
ficant t digit	0	0			TX = 0*	21	Test X = 0	Branch to address specified by second instruction word if $X = 0$. Otherwise, skip over second word.
ecimal lich is		0			TXF*	23	Test X < 1	Branch to address specified by second instruction word if $ X < 1$. Otherwise, skip over second word. (i.e. branch if X is a fraction.
hifted ficant		*			TXLT0*	22	Test X < 0	Branch to address specified by second instruction word if $X < 0$. Otherwise, skip over secon word.

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CLASS	SUBCLASS	MNEMONIC*	OCTAL OP CODE	FULL NAME	DESCRIPTION		
Branch	Count	IBNZ	31	Increment memory and branch if M ≠ 0	$M + 1 \rightarrow M$. If $M = 0$, skip second instruction word. Otherwise, branch to address specified by second instruction word.		
		DBNZ	32	Decrement memory and branch if $M \neq 0$	$M - 1 \rightarrow M$. If $M = 0$, skip second instruction word. Otherwise, branch to address specified by second instruction word.		
1/0	Multi-digit	IN*	27	Multidigit input to X	The processor supplies a 4-bit digit address $(DA4-DA1)$ accompanied by a digit address strobe (\overline{DAS}) for each digit to be input. The		
		σ		N	high order address for the number to be input would typically come from the second instruc- tion word. The digit is input on $D4-D1$, using ISEL = 0 to select digit data instead of in- structions. The number of digits to be input	8	3
					depends on the calculation mode (scientific notation or floating point) and the mantissa digit count (See Data Formats and Instruction Timing). Data to be input is stored in X and the stack is pushed $(X \rightarrow Y \rightarrow Z \rightarrow T)$. At the conclusion of the input, DA4-DA1 = 0.		
		OUT*	26	Multidigit output from X	Addressing and number of digits is identical to IN instruction. Each time a new digit address is supplied, the processor places the digit to be output on DO4-DO1 and pulses the R/\overline{W} line active low. At the conclusion of output, DO4-DO1 = 0 and DA4-DA1 = 0.		
1/0	Single-digit	AIN	16	Asynchronous Input	A single digit is read into the processor on D4– D1. ISEL = 0 is used by external hardware to select the digit instead of instruction. It will not read the digit until \overline{ADR} = 0 (ISEL = 0 selects \overline{ADR} instead of 15), indicating data valid. F2 is pulsed active low to acknowledge data just read.		
1/0	Flags	SF1 PF1	47 50	Set Flag 1 Pulse Flag 1	Set F1 high, i.e. F1 = 1. F1 is pulsed active high. If F1 is already high, this results in it being set low.		
	Q	SF2 PF2	51 52	Set Flag 2 Pulse Flag 2	Set F2 high, i.e. F2 = 1. F2 is pulsed active high. If F2 is already high, this results in it being set low.		
		PRW1	75	Pulse R/W 1	Generates R/W active low pulse which may be used as a strobe or to clock extra instruction bits into a flip-flop or register.	0	0
		PRW2	76	Pulse R/W 2	Identical to PRW1 instruction. Advantage may be taken of the fact that the last 2 bits of the PRW1 op code are 10 and the last 2 bits of the PRW2 op code are 01. Either of these bits can be clocked into a flip-flop using the R/W pulse.		
Mode Control		TOGM	42	Toggle Mode	Change mode from floating point to scientific notation or vice-versa, depending on present mode. The mode affects only the IN and OUT instructions. Internal calculations are always in 8-digit scientific notation.	0	0
		SMDC*	30	Set Mantissa Digit Count	Mantissa digit count is set to the contents of the second instruction word (=1 to 8).		
		INV	40	Inverse Mode	Set inverse mode for trig or memory function instruction that will immediately follow. Inverse mode is for next instruction only.	1	

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Note 1: instruct Note 2: Note 3: instruct Note 4: Note 5: executio for math

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cessor on D4-I hardware to ion. It will not EL = 0 selects ata valid. F2 is data just read.

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mory function follow. Inverse

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0000	0	TJC*	INV	XEY .
0001	1	TX=0*	EN	EX
0010	2	TXLTO*	TOGM	10X
0011	3	TXF*	ROLL	sa
0100	4	TERR*	SIN(SIN ⁻¹)	SORT
0101	5	JMP*	cos(cos ⁻¹)	LN
0110	6	OUT"	TAN(TAN-1)	LOG
0111	7 .	IN*	SF1	1/X
1000	8	SMDC*	PF1	YX
1001	9	IBNZ*	SF2	+ (M+)
1010	DP	DBNZ*	PF2	- (M-)
1011	EE	XEM	ECLR	x (Mx)
1100	CS	MS	RTD	. / (M/)
1101	PI	MR	DTR	PRW1
•1110	AIN	LSH	POP	PRW2
1111	HALT	RSH	MCLR	NOP

Note 1: HALT is same as NOP except it does not terminate number entry. External hardware must generate HOLD = 1 $\,$ to halt.

Note 2: ISEL = 0 for AIN, all 2-word instructions except SMDC.

Note 3: All instructions with 16 15 = 00, do not terminate number entry. Other instructions do terminate number entry.

INSTRUCTION MNEMONIC	EXECUTION TIME (MICROCYCLES) (AVERAGE)	EXECUTION TIME (MICROCYCLES) (WORST-CASE VALUES)	INSTRUCTION MNEMONIC	EXECUTION TIME (MICROCYCLES) (AVERAGE)	EXECUTION TIME (MICROCYCLES) (WOF.ST-CASE VALUES)	
0-9	1	238	OUT		583	
DP		152	IN		395	
EE	and the second second	151	SF1		163	
CS	The second second	166	PF1		185	
PI		1312	SF2	1941	163	
HALT		134	PF2		185	12.4
AIN	Service and and	284	PRW1	New York	130	12.5
TJC	·	208	PRW2		130	
TX=0	CONTRACTOR OF	278	SIN	56200	95900	959
TXLTO		197	COS	.56200	95900	959
TXF		277	TAN	35000	97600	e a 1
TERR		191	INVSIN	54000	93900	10.16
JMP		186	INV COS	54000	93900	
IBNZ		2314	INV TAN	30200	92900	-
DBNZ		2314	LN	24800	92000	
SMDC		163	LOG	30700	92600	1999
XEM	the state of the	812	EX	30800	93900	
MS	Selfit Services	839	10X	27400	96500	
MR		1385	+, -	2200	6600	
LSH		168	INV+, INV-	1700	5000	
RSH		173	(M+, M-)	- 1. C		
INV		166	x	3200	22700	
EN	State and	552	INV x (MX)	2700	21400	
TOGM	1.	157	1	7800	22300	
ROLL		905	INV / (M/)	7300	21100	
ECLR	NA STREET	163	1/X	4500	22800	
POP	THE REAL PROPERTY.	448	YX	55400	95500	
MCLR		734	SORT	7000	30200	2302m
XEY		652	sa	3000	21900	
NOP		122	DTR, RTD	9600	41700	

TABLE V. Instruction Execution Times

Note 1: All times are measured from leading edge of ready for first word of the instruction to leading edge of ready for first word of the next instruction.

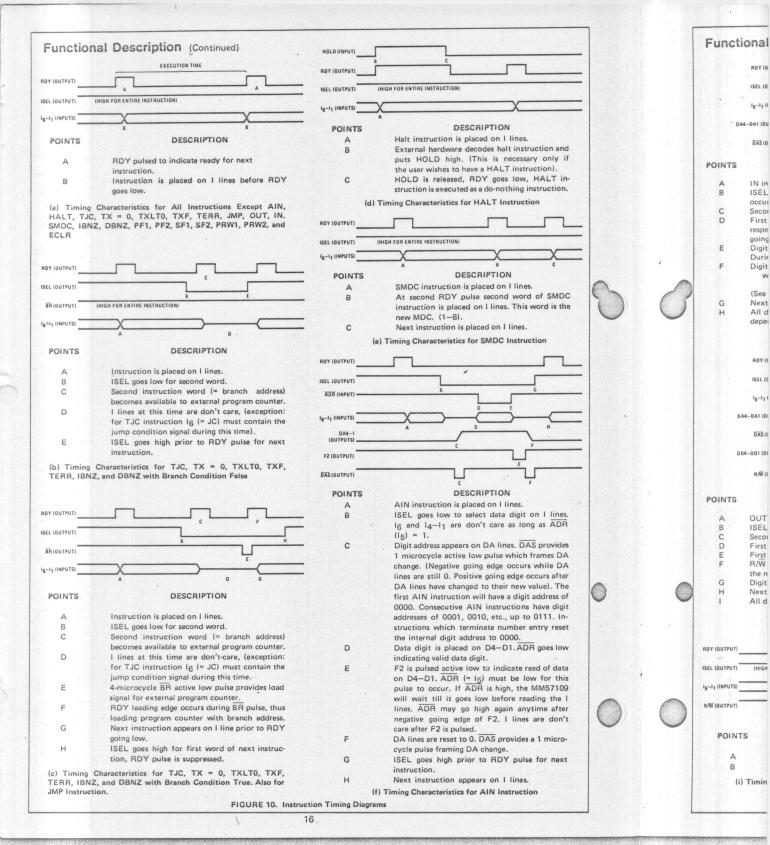
Note 2: Add 67 microcycles to the execution time of any instruction which initiates number entry and is preceded by an ENTER instruction. Note 3: Add 282 microcycles to the execution time of any instruction which initiates number entry and is not preceded by an ENTER instruction.

Note 4: Add 1003 microcycles to the execution time of any instruction which terminates number entry.

Note 5: The execution time of each instruction is a function of the internal state of the device. It is not possible to predict precisely what the execution time will be for any given instruction. This table shows worst-case values for basic instructions, and both average and worst-case values for mathematical instructions.

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10 ms = 4



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<complex-block><pre> function is a serie of the serie</pre></complex-block>	And methods in the second provide the second pro	A reference of the second representation o	lines. t instruction and ecessary only if instruction). low, HALT in- hing instruction.		נס				c									
<form></form>	An information of a start of a	And reactions of the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due significant work is the second data section work. Due second data section work is the second data section work. Due second data section work is the second data section work. Due second data section work is the second data section work. Due second data section work is the second data section work. Due second data section work is the second data section work. Due second data section work is the second data section work is the second data second data section work is the second data second data section. Due second data s	lines. Instruction and ecessary only if Instruction). Iow, HALT In- ing instruction.		La Contra C	16-11 (INPUTS)								1			-	-
<form><pre>purpued of the second of</pre></form>	The interface of the former of the former of the interface of the inter	The function and decay of if it is the post of it is the control is the set of it is the post of it is the control is	instruction and cessary only if instruction). low, HALT in- ing instruction.		DA		X	8	>		X	X	X	X	X	X		_
<complex-block> POINTS DEMINITAL 9 N. H. M. M.</complex-block>	A strategy of y figures that has been reading to the strategy of y figures and ready of the strategy of y figures that has been reading to the strategy of y	Balance is and iteration and service of the service is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is placed on 1 line. Control is a single-offer and iteration is p	instruction and cessary only if nstruction). ow, HALT in- ing instruction.		A CONTRACTOR OF A CONTRACTOR OFTA CONT	A4-DA1 (OUTPUTS)	A			E	-x	- C	ý	- x	-x	- Y	7	1.1
<complex-block> POINTS DEMUTIVE 9 Numerical end end end end 9 Numerical end end end end end 9 Numerical end end end end end end end end end end</complex-block>	VINITY DESCRIPTION OF A DESCRIPTION A DESCRIPTION A DE	PUNT PUNT DESCRIPTION A PUNT PUNT DESCRIPTION A PUNT PUNT DESCRIPTION A PUNT PUNT DESCRIPTION A PUNT PUNT DESCRIPTION A PUNT PUNT DESCRIPTION PUNT PUNT DESCRIPTION PUNT	cessary only if nstruction). low, HALT in- ing instruction.		1.1.1.1.1.1	DAS (OUTPUT)				Ů	-ú-	Ú	Ú	-ú-	-ú	Ú	-J	-
<form> A. M.N. M. M.</form>	 A. Nichowski, S. S.	 A Hearcoon based on line. A Hearc	ow, HALT in- ing instruction.		BOINTS						-	DESCR	IPTION					
 B. ISEL gosts for second instruction word. Data digits multiplexed onto l lines when ISEL = 0. I lines are don't care until DAS pulse constrained in the control of a second word of instruction becomes available to external hardware as high-order address for a RAM or other device. B. Foti digit address appears on DA lines in the digit address is 0 or 2 depending on whether model is floating point or externitie motation, and order address for a RAM or other device. B. Digit data becomes to next digit, is 0, 1, 2, 9,, N.H floating point or 2, 3, 4,, N.H scientific notation. Whether model and the second is read. During this time data is read. B. Digit address convert digit, is 0, 1, 2, 9,, N.H floating point or 2, 3, 4,, N.H scientific notation. When N = MOC 2010. Spin which is microcycle after DAS negative edge. Digit data meanix valid out of the DAS pulse. During this time data is read. B. Next digit is placed on O4-Di, agin which is microcycle after DAS negative edge. Digit data sciences are alia. Digit Address gost 0000. SEL gost high bulks for next instruction. Number of digits read deends on notation and manisa digit count (see Data Formati). B. Otto science and in. Digit Address gost 0000. SEL gost high bulks for next instruction. Number of digits read deends on rotation is placed on 14 microcycle after DAS negative edge. Digit data sciences are alia. Digit Address post DAS DIME. POINTS DESCRIPTION A. OL T instruction is placed on 11 lines. B. B. Gost DM or of restruction is placed on 11 lines. B. B. Gost DM or of restruction is placed on 11 lines. B. B. Gost DM or of restruction is placed on 14 microcycle after the negative edge. DAS negative edge. DAS negative edge. The split address are noted to the transmission of the split address are noted to the split address are noted address. B. Otto instruction is placed on 14 microcycle after the negative edge of DAS. The split address are no	 B Bill Less low for second instruction word. Data digit multiplexed oncel laws when DSE = 0.1 lines are don't care with DSE public documents are high-order address in the ARAM or other docid. B Bill Less low for second instruction words. Data digits multiplexed oncel lines are don't care with DSE public documents are high-order address in the ARAM or other docid. C Bill Less low for second instruction words. The high address is the power gets document are with a second instruction words. The high address is the power gets document are with a second instruction words. The high address is the power gets document are with a second instruction words. The high address is the power gets document are with a second instruction words. The high address is the power detail document are with a second instruction words. The high address is the power detail document are with a second instruction words. The high address is the power detail document are with a second instruction words. The high address is the power detail document are with a second instruction. The high address is the power detail document are with a second instruction. The high address is the power detail document are with a second instruction. The high address is the power detail document are with a second instruction. The power detail document are with a second instruction and the power detail document and the power detail document are with a second instruction. The power detail document are with a second instruction and the power detail document are with a second instruction and the power document are with a second instruction. The power details are with a second instruction and the power document are with a second instruction and the power document are with a second instruction and the power document are with a second instruction and the power document are with a second instruction and the power document are with a second instruction and the power document are with a second instruction and the power document are with	 Big BinDecidion. BinDecidion. Bin			1.	IN instructio		ad on 1 li				DESCH	IF HON					
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	FIGURE 10. Instruction Timing Diagrams (Continued)	FIGURE 10. Instruction Timing Diagrams (Continued)														1000	SF2 Instruc	tions
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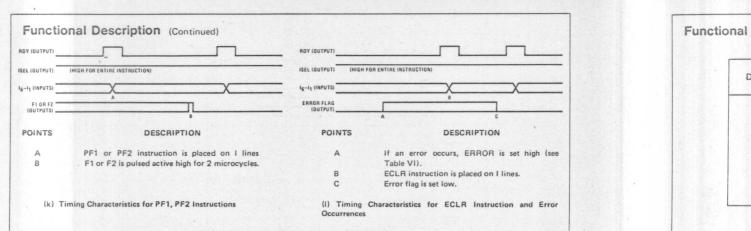


FIGURE 10. Instruction Timing Diagrams (Continued)

DATA FORMATS

IN/OUT Instructions

Mantissa digit count and notation mode determine data format. Table VII shows the contents of the DA and DO lines for an IN or OUT instruction. Anywhere from 4 to 11 digits will be input or output by a single instruction.

AIN Instruction

One digit is input per AIN instruction. A maximum of 8 digits may be entered into the X mantissa by using consecutive AIN instructions. Digit entry is terminated by EN or any function instruction. Table VII shows the DA lines for consecutive AIN instructions.

ERROR CONTROL

The error flag, which can drive an LED indicator, is set high upon detection of an arithmetic or output error. (See Table VI).

TABLE VI. Error Conditions

Error flag is set when:

1. LN X when $X \leq 0$ LOG X

- 2. Any result $< 10^{-99}$ Any result $\ge 10^{100}$
- 3. TAN 90°, 270°, 450°, etc.
- 4. SIN X, COS X, TAN X when $|X| \ge 9000^{\circ}$
- 5. SIN⁻¹ X, COS⁻¹ X when |X| > 1 or $|X| \le 10^{-50}$
- 6. SQRT X when X < 0
- 7. /, INV/, 1/X when X = 0
- 8. In floating point mode OUT instruction if number of mantissa digits to left of decimal point is > Mantissa Digit Count.

The error flag can be tested by the TERR instruction (which branches if ERROR = 1) or it can be used to clear the external program counter, resulting in a hardware jump to location 0, the error recovery location. In either case, an ECLR instruction must be executed to clear the error flag.

For automatic error recovery, ERROR is wired to the asynchronous clear input of the external program counter (PC). The instruction at location 0 is an ECLR to clear ERROR so that the next RDY pulse will advance the PC to location 1. A JMP instruction at location 1 with the address at location 2 of an error routine is then executed, which results in a transfer of program control to the error routine. These first 3 error recovery locations are skipped over upon reset (POR) as can be seen in the initialization and instruction fetch flowcharts. The program shown in Table VIII shows typical error recovery coding.

SAMPLE SYSTEMS

Figures 11-14 show sample systems using the MM57109. Figure 11 shows a simple demonstrator system using switches to enter instructions. An LED display is used to demonstrate the OUT instruction, with a switch to force an OUT instruction on the I lines and to hold the HOLD input low for 1 second for repeated execution of the OUT instruction, resulting in a multiplexed display. A flip-flop latches the $\overline{\text{BR}}$ pulse which occurs when a test and branch instruction is true. LED lamps provide visual indication of the various flags. An enter button allows single instruction words to be entered one at a time.

Figure 12 shows a stand-alone system with external program counter and a RAM to expand memory.

Figure 13 shows the MM57109 used as a microprocessor peripheral. Latches contain instructions for the MM57109 and digit data for the microprocessor.

Figure 14 shows a data acquisition system which obtains data from a 3-digit A/D converter.

Figure 15 shows a microprocessor to MM57109 interface using 2 FIFO's for instruction and data buffering.

These sample systems are not intended to be detailed drawings of a complete system (except Figure 11). Their purpose is to provide the designer with some ideas as to how to use the MM57109 in an actual system.



OCTAL ADDI

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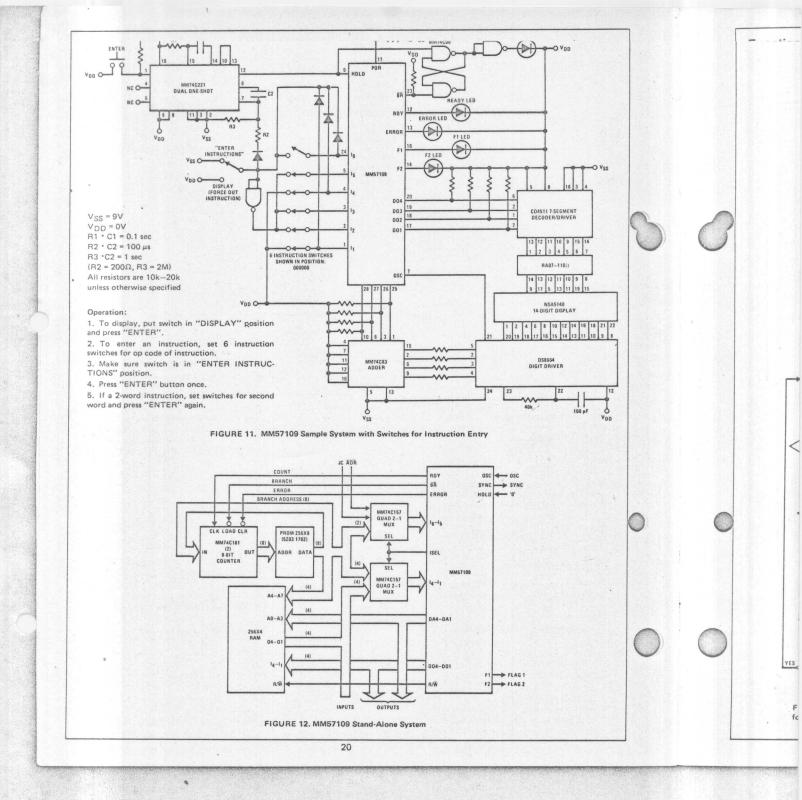
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		Functiona	al Desci	ription (Co			VII. Data Form s (a) Mode = Sci			а. 	
			DA4-DA	.1	IN: OUT:	D4 D04	D3 DO3	D2 D02	D1 D0		
_			0			Most signi	ficant exponer	t digit			
See			2 3 4			Sm Not used - Most signi	0 ficant mantissa	0 digit (Decim	Se nal point f		s digit)
			:			•					
ror		L	MDC + 3	3			ficant mantissa tions (b) Mode =				
						IN:	D4	D3	D2		01
0	0		DA4-	DA1 D	P POS	OUT:	DO4	DO3	DO2		01
0	0		2334	3	11 10		Sm DP POS Most signific	0 ant Mantissa (0 Digit = 0—		0
			:		:		:				
-			MDC	+ 3 12	- MDC		• Least signific	ant Mantissa	Digit = 0-	-9	
			Sm = Se =	 Mantissa digit Sign of mantis Sign of expone Decimal point 	ssa, 0 = posit ent (Se = 0 i t position in	tive, 1 = neg in floating p ndicator is a	ative oint mode) value in the ran	ge from 11 dov			
			MDC = Sm = Se =	 Sign of mantis Sign of exponent Decimal point 	ssa, 0 = posit ent (Se = 0 i t position in	tive, 1 = neg in floating p ndicator is a the DP POS	ative oint mode)	ge from 11 dov			
			MDC = Sm = Se = DP POS =	 Sign of mantis Sign of expone Decimal point cates a digit, a 	ssa, 0 = posit ent (Se = 0 i t position in	tive, 1 = neg in floating p ndicator is a the DP POS	ative oint mode) value in the ran column in the ta	ge from 11 dov			
			MDC = Sm = Se = DP POS =	 Sign of mantis Sign of expone Decimal point cates a digit, a of this digit. 	ssa, 0 = posit ent (Se = 0 i t position in	tive, 1 = neg in floating p ndicator is a the DP POS AIN	ative oint mode) value in the ran column in the ta	ge from 11 dow ble. The decima	al point is lo	ocated to the	
			MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponit Decimal point cates a digit, a of this digit. 	ssa, 0 = posit ent (Se = 0 i t position in	tive, 1 = neg in floating p ndicator is a the DP POS AIN	ative oint mode) value in the ran column in the ta Instruction	ge from 11 dow ble. The decima	al point is lo	ocated to the	
			MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 	ssa, 0 = posi ent (Se = 0 i t position in as given by	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas	ative oint mode) value in the ran- column in the ta Instruction t significant dig t significant dig	ge from 11 dow ble. The decima git Xm (first A git Xm (eight)	AIN instru	ction)	
			MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 	ssa, 0 = posii ent (Se = 0 i t position in as given by given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa.	ative oint mode) value in the ran- column in the ta Instruction t significant di t significant di Decimal point fo	ge from 11 dow ble. The decima git Xm (first A git Xm (eight)	AIN instru	ction)	
	•		MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 Note, X₁ 	ssa, 0 = posii ent (Se = 0 i t position in as given by given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos	ative oint mode) value in the ran column in the ta Instruction t significant di t significant di Decimal point fo Error Recovery	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) silows last digit Coding	AIN instru	ction)	
	•	OCTAL AD	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 	ssa, 0 = posii ent (Se = 0 i t position in as given by given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative oint mode) value in the ran- column in the ta Instruction t significant di t significant di Decimal point fo	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) silows last digit Coding	AIN instru AIN instru entered.	ction)	
		00 01	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 Note. X, OCTAL OP CODE 53 25 	ssa, 0 = positi ent (Se = 0 i t position in as given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative oint mode) value in the ran- column in the ta- Instruction t significant di t significant di Decimal point fo Error Recovery NSTRUCTIOI	ge from 11 dov ble. The decima git Xm (first A git Xm (eight) sllows last digit Coding	AIN instru AIN instru entered.	ction) truction) Clear err Jump to	COMMENT
		00	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, of this digit. 4-DA1 0 7 Note. X, OCTAL OP CODE 53 	ssa, 0 = positi ent (Se = 0 i t position in as given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative oint mode) value in the ran- column in the ta- Instruction t significant dig t significant dig Decimal point for Error Recovery NS TRUCTION MNEMONIC ECLR	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) lollows last digit Coding	AIN instru AIN instru entered.	ction) truction) Clear err Jump to	comment
	•	00 01 02	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 Note. X, OCTAL OP CODE 53 25 	ssa, 0 = positi ent (Se = 0 i t position in as given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative pint mode) value in the ran- column in the ta- Instruction t significant dia t significant dia Decimal point for Error Recovery NS FRUCTION MNEMONIC ECLR JMP	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) lollows last digit Coding	AIN instru AIN instru entered.	ction) truction) Clear err Jump to	COMMENT
	0	00 01 02 03	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 Note. X, OCTAL OP CODE 53 25 	m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative pint mode) value in the ran- column in the ta- Instruction t significant dia t significant dia Decimal point for Error Recovery NS FRUCTION MNEMONIC ECLR JMP	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) lollows last digit Coding	AIN instru AIN instru entered.	ction) truction) Clear err Jump to Address	COMMENT ror flag error routine of label 'ERROF
	•	00 01 02	MDC = Sm = Se = DP POS =	 Sign of mantis Sign of exponential point cates a digit, a of this digit. 4-DA1 0 7 Note. X, OCTAL OP CODE 53 25 	ssa, 0 = positi ent (Se = 0 i t position in as given by m = X regist	tive, 1 = neg in floating p ndicator is a the DP POS AIN Mos Leas ter mantissa. TABLE VIII.	ative pint mode) value in the ran- column in the ta- Instruction t significant dia t significant dia Decimal point for Error Recovery NS FRUCTION MNEMONIC ECLR JMP	ge from 11 dow ble. The decima git Xm (first A git Xm (eight) lollows last digit Coding	AIN instru AIN instru entered.	ction) truction) Clear err Jump to Address	COMMENT



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