Complex Standards

MM5311,MM5312,MM5313,MM5314, digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (four or six digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11 to 19V and do not require a regulated supply. The MM5311 through MM5314 clocks are packaged in 24 and 28 lead dual-in-line packages.

features

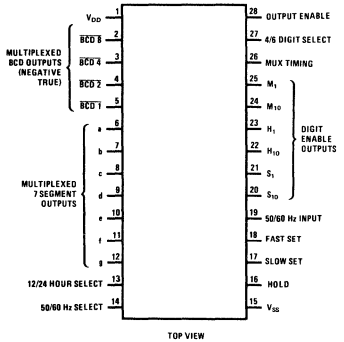
- 50 or 60 Hz operation
- 4 to 6 digit display mode
- 12 or 24 hour display format
- Leading-zero blanking (12-hour format)
- $\overline{BCD}$ and 7-segment outputs
- Single power supply
- Fast and slow set controls
- Output enable control
- Internal multiplex oscillator
- Hold count control

applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks

connection diagrams

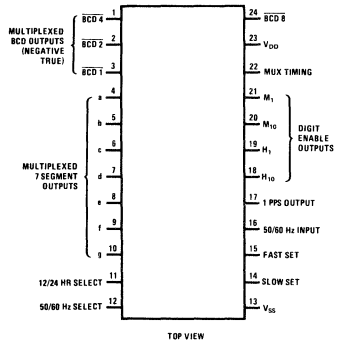
Dual-In-Line Package



TOP VIEW

Order Number MM5311D See Package 7 **Order Number MM5311N** See Package 19

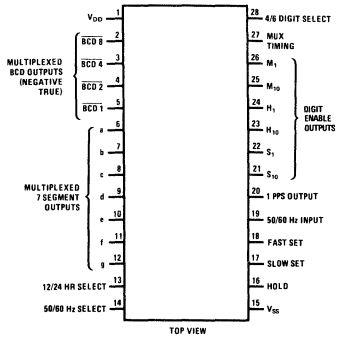
Dual-In-Line Package



TOP VIEW

Order Number MM5312D See Package 6 **Order Number MM5312N** See Package 18

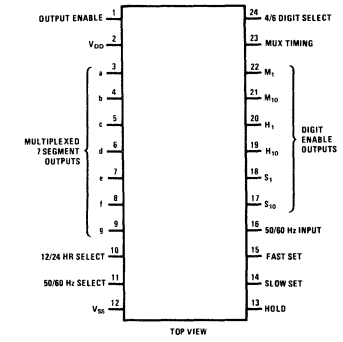
Dual-In-Line Package



TOP VIEW

Order Number MM5313D See Package 7 **Order Number MM5313N** See Package 19

Dual-In-Line Package



TOP VIEW

Order Number MM5314D See Package 6 **Order Number MM5314N** See Package 18

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = +14V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11	14	19	V
Power Supply Current	V_{SS} = +14V (No Output Loads)		8.0	15	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS} − 2.0	V_{SS} − 1.0	V_{SS}	V
Logical Low Level		−2.0	0	4.0	V
Multiplex Frequency	Determined by External R & C	dc	1.0	60	kHz
All Logic Inputs					
Logical High Level	Internal 20kΩ Resistor to V_{SS}		V_{SS}		V
Logical Low Level		−2.0	0	4.0	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2kΩ to V_{DD}	2.0	5.0	20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100Ω to V_{SS}	5.0	10.0	25	mA sink

functional description

A block diagram of the MM5311 thru MM5314 digital clocks is shown in Figure 1. The various functional capabilities of the clocks are listed in Table 1. Connection diagrams for these devices are shown on page 1. The following discussions are based on Figure 1.

50 or 60 Hz Input: This input is applied to a Schmitt trigger shaping circuit which provides approximately five volts of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in Figure 10 should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the time keeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1-pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 20 kΩ pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in Figure 1, the prescale counter provides both 1-pps and 10-pps signals. As shown in Table 1, the MM5312 and MM5313 clocks provide the 1-pps signal as an output. On these clocks, the 10-pps signal (in place of the 1-pps signal) may be selected as an output via a lead-bonding option.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal 20 kΩ pull-up resistors provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain (Figure 1) are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷ 50 or ÷ 60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷ 60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷ 60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24 Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal 20 kΩ pull-up) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a six-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6 digit select

functional description (con't)

input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{BCD}$ and 7-segment. The sequential output order is from digit-6 (unit seconds) thru digit-1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in Figure 2. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in Figure 10) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the schmitt trigger in Figure 2. Figure 3 provides guidelines for selecting the external components relative to desired multiplex frequency. Figure 4 illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as the 50 or 60 Hz input.

4 or 6 Digit Select Input: Like the other control inputs, this input is provided with an internal 20 kΩ pull-up resistor. With no input connection the clock outputs data for a 4 digit display. Applying V_{DD} to this input provides a 6 digit display (not applicable to the MM5312 clock, see Table 1).

Output Enable Input: With this pin unconnected the $\overline{BCD}$ and 7-segment outputs are enabled (via an internal 20 kΩ pull-up). Switching V_{DD} to this input inhibits these outputs.

Output Circuits: Figure 5-A illustrates the circuit used for the $\overline{BCD}$ and 7-segment outputs. Figure 5-B shows the digit enable output circuit. Figure 6 illustrates interfacing these outputs to standard and low-power TTL. Figures 7 and 8 illustrate methods of interfacing these outputs to common-anode and common-cathode LED displays, respectively. A method of interfacing these clocks to gas-discharge display tubes is shown in Figure 9. When driving gas-discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. Figure 9 also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

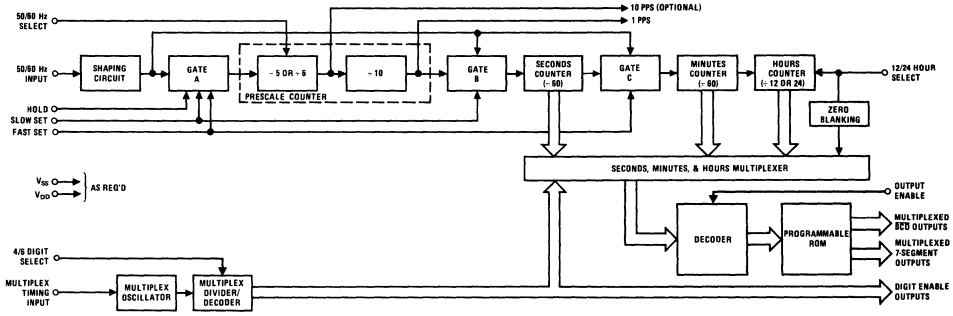


FIGURE 1. MM5311 thru MM5314 Digital Clocks, Block Diagram

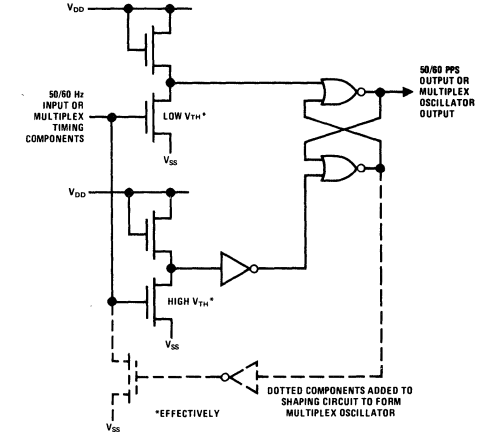


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

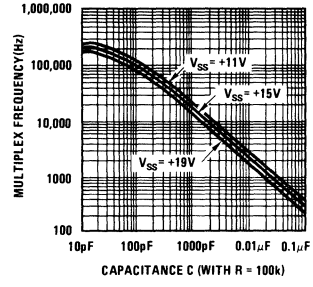
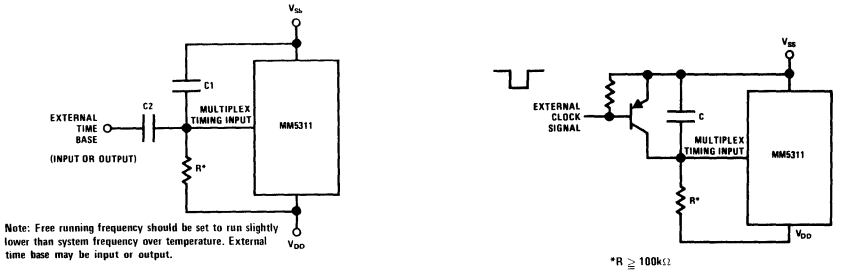


FIGURE 3. Multiplex Timing Component-Selection Guide

functional description (con't)



Note: Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.

FIGURE 4. Synchronizing or Triggering Multiplex Oscillators

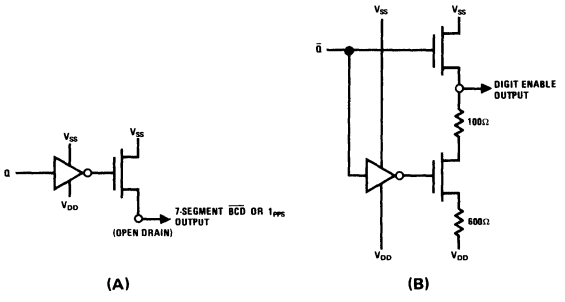


FIGURE 5. Output Circuits

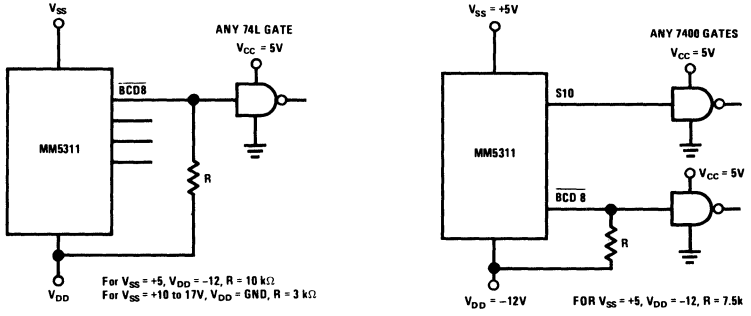
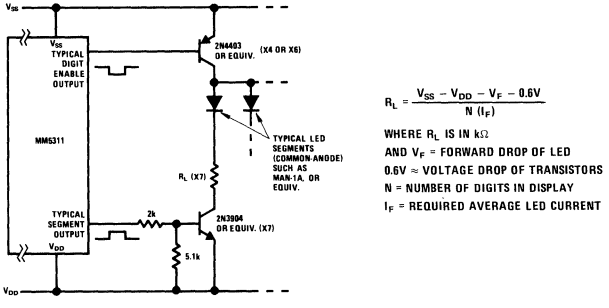


FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} - V_{DD} - V_F - 0.6V}{N\ (I_F)}$$

WHERE R_L IS IN kΩ
AND V_F = FORWARD DROP OF LED
0.6V ≈ VOLTAGE DROP OF TRANSISTORS
N = NUMBER OF DIGITS IN DISPLAY
I_F = REQUIRED AVERAGE LED CURRENT

FIGURE 7. Interfacing Common-Anode LED Displays

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functional description (con't)

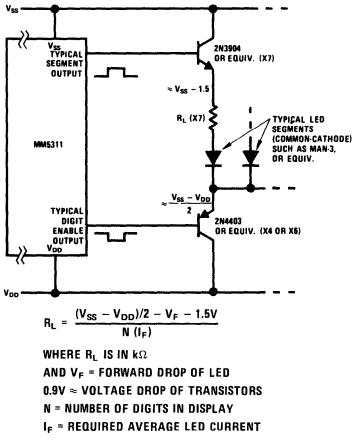

FIGURE 8. Interfacing Common-Cathode LED Displays

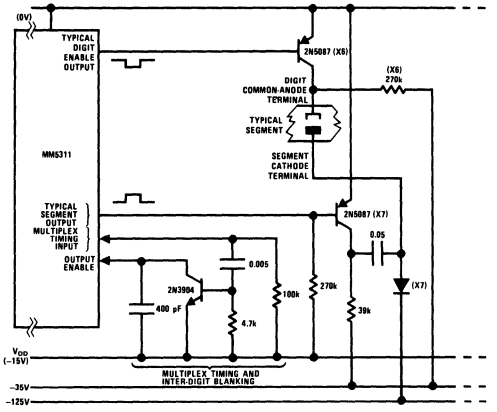

FIGURE 9. Interfacing Panaplex II* Neon Display Tube

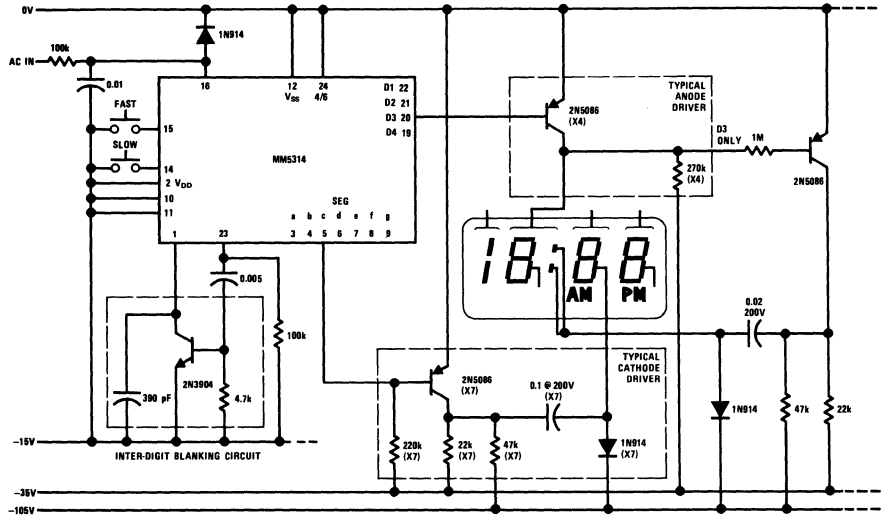

FIGURE 10. MM5314AN Driving Gas-Discharge Display, Typical Application

*TM of Burroughs Corp.