## DOUBLE-CLOCKING CUTS STANDARD REGISTERS TO NON-STANDARD SIZES

### INTRODUCTION

It may be more economical to make a standard MOS register appear shorter, logically, than to have a special register made to order. A double-clocking technique uses up the unwanted length by causing input bits to be stored twice and then to be read out as individual bits when they reach the end of the register.

Figure 1 shows the clock format. A double clock applied for N of the normal input data intervals at a fixed portion of the total recirculation time

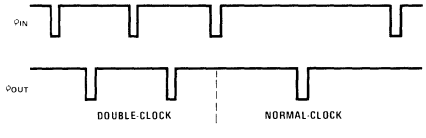


**FIGURE 1. Clock rate is doubled for N data input periods to make the register appear shorter by N bits, and then resumes normal frequency.**

will shorten the register by N stages and clock periods. If N is 2, a 1-0 input data sequence would be stored as 1-1-0-0. Since these appear as the output at the time the clock is again doubled, the output gate only detects 1-0.

Suppose a parallel array of eight 1991-bit registers is needed to store 1991 8-bit words in a buffer memory. Each could be a subassembly as in Figure 2. The MM5013 and MM5016 are standard 1024-bit and 512-bit register and the MM5019 is mask-programmed to order in sizes up to single 512 or dual 256-bits.

The design in Figure 3 provides the same length with two MM5013 registers. The eight registers are assembled with 16 instead of 24 packages.

Also, the second MM5013 costs less than an MM5016/MM5019 combination (the longer the register the less the cost per bit). The only addition to overhead logic is the decoder and dual clock generator formed with the logic in the dotted lines—one DM7473 dual J-K flip-flop and half a package each of DM7400 and DM7420 gates.

In the example, N = 2048 − 1991, or 57. Therefore, the registers should be clocked at double frequency for the first 57 data periods of the recirculation time. The extra logic decodes the bit-counter output and generates the 114 clocks needed.

There are some limitations to this technique. Obviously, the normal rate should not be more than half the maximum clock rate for the registers

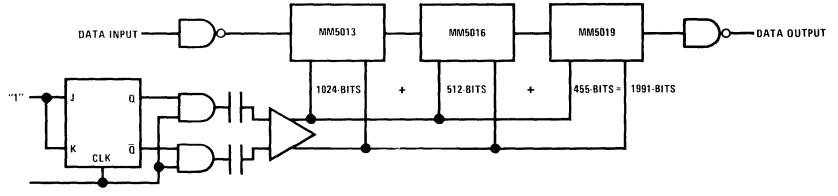


**FIGURE 2. Mask-programmable MM5019 register may be used to assemble odd-length registers.**

used. Also, if too many bits are subtracted, the clock-drive loading may be affected adversely. The driver power requirement is proportional to average frequency. In the example, it is increased by f(2048/1991) or 2.8%, which has little effect. But if an MM5016 was shortened from 512 to 397 bits, the increase in power would be 28%. In this case, instead of shortening the MM5016, it may be more practical to order an MM5019 at the desired length. At still shorter lengths, the MM5007 mask-programmable dual 100-bit programmable register should be considered. Generally speaking, double-clocking becomes more cost-effective when the system register length is long.

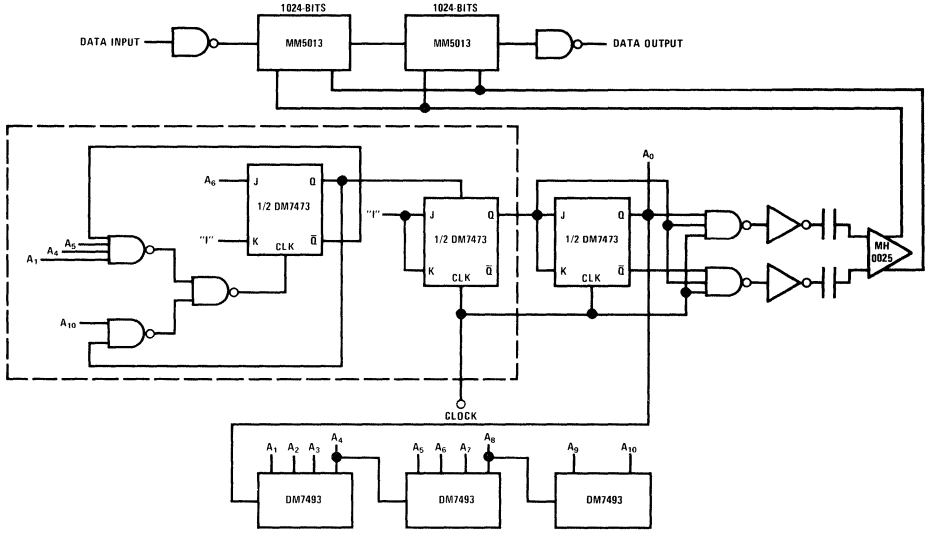


FIGURE 3. A 2048-bit register is made to appear only 1991 bits long by the logic within the dotted lines.