MASK PROGRAMMING SPECIALIZES MOS SHIFT REGISTER DESIGNS

A quick, economical way of customizing MOS shift register bit lengths is programming the metallization mask, the mask that defines the thin-film wiring pattern etched on the silicon wafer. Metallization etching is the most convenient process step to specialize because it is consistent from wafer to wafer and is the last major process step before testing.

Utilizing this technique, National Semiconductor has developed two variable-length dynamic MOS register designs. Both of them, MM4007/MM5007 and MM4019/MM5019, are bipolar compatible. Dual registers 20 to 256 bits long, single registers 40 to 512 bits long, and a variety of taps and pinouts provide the system designer with a method of obtaining custom length shift registers quickly and at reasonable cost.

Up to metal masking, wafer design and fabrication are standardized. No time is lost—or money spent—in developing custom arrays or tuning up the process. Automatic test systems further reduce turnaround time and production costs.

Programming the metallization mask mainly involves routing signal connections past selected storage cells to adjust total register length to the desired number of cells. Wire-bonding changes provide output tap options.

DUAL REGISTER DESIGNS

Basically, each of the variable-length types is a dual register (Figure 1 and Table 1A).

There are enough storage cells, I/O stages, clock and power supply lines on each MM4007 chip to make up to two 100-bit registers. The minimum length of each register half, M_A and M_B, is 20 bits. The programmable parts, P_A and P_B, may be 0 to 80 bits long. Lengths need not be equal. For instance, register A may be 29 bits and register B 76 bits (P_A = 9, P_B = 56).

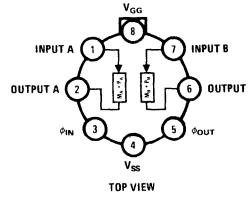


FIGURE 1. Dual Shift Registers

An MM4019/MM5019 chip is similarly organized, except that M_A and M_B are 40 bits and P_A and P_B vary from 0 to 216 bits. Again, lengths may be unequal, such as 240 bits in the A half and 136 bits in the B half.

Clock and supply line pin locations are standardized, but I/O pinouts are selectable. The I/O terminals on the chip may be bonded to package pins which are more convenient for the PC board layout. For example, a couple of board feedthroughs might be eliminated by bonding the A register input to Pin 7 (rather than Pin 1) if data comes in from the right and exits on the left. Or, A and B could share an input pin when they have the same signal source.

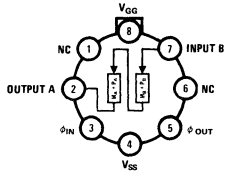
TABLE 1 Register Length Options

	MM4007/MM5007			MM4019/MM5019		
	M (BITS)	P (BITS)	TOTAL (BITS)	M (BITS)	P (BITS)	TOTAL (BITS)
A. DUAL REGISTERS						
A Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B. SINGLE REGISTERS	$M_A + M_B$	$P_A + P_B$		$M_A + M_B$	$P_A + P_B$	
	40	0 to 160	40 to 200	80	0 to 432	80 to 512
C. TAPPED SINGLE REGISTERS Total register length same as single registers with tap locations determined by either half of the dual registers.						

SINGLE-REGISTER OPTIONS

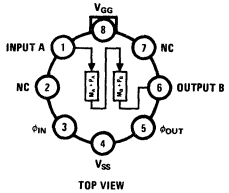
Since clock rates are synchronized by the common clock inputs, the registers may also be serially connected inside the package, as diagrammed in Figure 2. One output is internally connected to the other input.

This extends the maximum length of an MM4007/MM5007 to 200 bits and the MM4019/MM5019 maximum to 512 bits. However, each half still has the same minimum, so the minimums become 40 and 80 bits, respectively (Table 1B). Again, the customer specifies the most convenient I/O pin connections.



TOP VIEW

FIGURE 2a

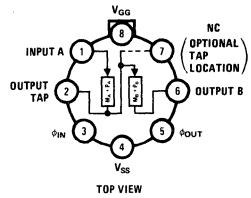


TOP VIEW

FIGURE 2b

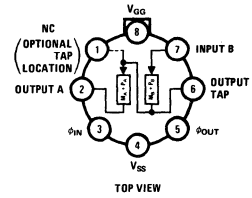
FIGURE 2. Single Registers

Going to the output tap designs of Figure 3 takes only one more wire bond; from the first register output to any available pin. Tap locations are selected by specifying the bit lengths of each of the dual registers. For example, an MM5007 105 bits long may be tapped at any stage from 20 to 85 bits. Generally, this flexibility makes input taps unnecessary—an output at 29 bits in a 105-bit register usually serves the same purpose as an input at 76 bits.



TOP VIEW

FIGURE 3a



TOP VIEW

FIGURE 3b

FIGURE 3. Output Tap Options

OPERATING CHARACTERISTICS

All specifications, except bit lengths, are the same as those of other MM4000/MM5000 series dynamic shift registers with the same number of I/O stages.

Clock-line capacitance, power dissipation, as well as other AC and DC parameters, are independent of the lengths programmed. This is accomplished by standardizing clock and supply wiring patterns to achieve minimum turnaround time and cost.

The MM4007/MM5007 and MM4019/MM5019 are fabricated using a low-threshold, p-channel enhancement-mode technology developed for the MM4000/MM5000 series of registers. This means that they are bipolar compatible, sensing TTL or DTL data without input pull-up resistors and driving TTL or DTL loads without output pull-down resistors. They operate on standard +5V and −12V supplies. The clock frequency range is also the same, from 300 Hz to 2.5 MHz, guaranteed.

Either TO-99 or dual-in-line packages may be specified. MM4007 and MM4019 operate at −55°C to +125°C. MM5007 and MM5019 are commerical types, specified for −25°C to +70°C.