A SIMPLE POWER SAVING TECHNIQUE FOR THE MM5262 2k RAM

INTRODUCTION

The MM5262 is a state of the art RAM designed to operate efficiently in modern bus organized systems. Most bused systems present the address information to the data bus only during the early portion of the machine cycle and then transfer data during the remainder of the cycle. The MM5262, unlike many other RAMs, does not need a memory address register to hold the address stable on its inputs during the complete cycle because the address is clocked into the MM5262 on-chip address register by Phase 1. The address and chip select signals need only be applied during Phase 1 and the Phase 1 to Phase 2 gap.

SAVING POWER

Because of the very low power dissipation of the MM5262 when the clocks are turned off (< 2.0 mW), a method for decoding the clocks of unselected chips in the memory array would result in a sizable decrease in power consumption. A problem arises because to deselect a chip, a Phase 1 pulse must be applied to clock the disable signal into the chip. There would be little advantage in allowing Phase 1 to free run and decoding only Phase 2 and Phase 3 because approximately 75% of the power dissipation is associated with Phase 1. The best solution is a decoding arrangement where the disabling of Phase 1 is delayed by one cycle and the enabling of Phase 1 is not delayed. The chip will receive one extra Phase 1 pulse to disable it and will no longer draw power until it is again enabled. The power then becomes worst case when alternately accessing two chips. Both chips will draw power continuously while all other deselected chips draw 0.1 mA each. Table I shows expected power supply currents for various size memories per bit of word width: column II – average power supply current with only one chip selected; column III – average power supply current under worst case conditions of alternately selecting two chips; and column V – worst case average current including refresh (assuming a 635 ns cycle time). The peak current during refresh, assuming all chips are refreshed at the same time, is equal to the total number of chips multiplied by 20 mA maximum per chip. During an interval of 2.0 ms, the memory will cycle almost 3,000 times, of which only 32 cycles must be devoted to refresh; therefore, the average refresh power will be one percent of the peak power or 0.2 mA per chip. Comparable savings in clock driver power dissipation are also realized.

Using the data from Table I for a common application, such as an 8k-by-16 memory for a minicomputer, the power is cut to half that required without decoding. In a large memory, such as 64k words, the power is cut by a factor

TABLE I.

NUMBER OF WORDS	CHIPS PER BIT OF WORD WIDTH	MAXIMUM POWER SUPPLY CURRENT (mA)/PER BIT OF WORD WIDTH					
		I NO CLOCK DECODING	II CLOCK DECODING ONE CHIP SELECTED	III CLOCK DECODING TWO CHIPS ALTERNATELY SELECTED	IV ADDITIONAL AVERAGE REFRESH CURRENT	V NS TOTAL WORST CASE	6003 (4 mA STANDBY CURRENT)
2,048	1.0	20				20	10
4,096	2.0	40	20.1	40	0	40	20
8,192	4.0	80	20.3	40.2	0.4	40.6	28.2
16,384	8.0	160	20.7	40.6	1.2	41.8	44.6
32,768	16	320	21.5	41.4	2.8	44.2	77.4
65,536	32	640	23.1	43	6.0	49	143
131,072	64	1,280	26.3	46.2	12.4	58.6	274

N = Number of words in 2048 increments N $\geq$ 4096
B = Number of bits/words
t_{CYCLE} = Memory cycle time

$$\underbrace{I_{DD}\,(AVG)_{MAX}}_{V} = B\Bigg\{\underbrace{2 \times 20 + \left(\frac{N}{2048} - 2\right) \times 0.1}_{III} + \underbrace{\left(\frac{N}{2048} - 2\right) \times \frac{32\,t_{CYCLE}}{2\text{ ms}} \times 20}_{IV}\Bigg\}$$

of 13. Figure 1 shows a plot of memory current as a function of memory size with a comparison of the nearest equivalent 2k RAM.

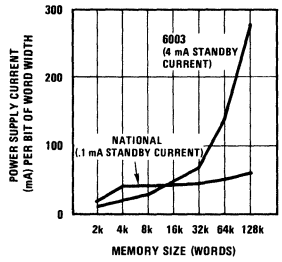

FIGURE 1. Memory Size vs 2k RAM Power Supply Current

A memory system configured as 8k words by 16-bits per word, for example, would draw 80 mA times 16-bits (1.28 Amps) if undecoded. If the same memory is decoded, the current drops to 40.6 mA times 16-bits (650 mA) which is half the current of the undecoded memory. In a large system, such as 64k words by 32-bits per word the savings is even greater. Undecoded the supply current is 640 mA times 32-bits (20.5 Amps) while the same memory when the clocks are decoded draws 49 mA times 32-bits (1.6 Amps). The power for the decoded memory then is one-thirteenth of that required for the undecoded memory.

LOGIC IMPLEMENTATION

Figure 2 shows the logic required to implement the power saving technique, Figure 3 is a timing diagram for the logic, and Figure 4 is a block diagram of an 8k word by 16-bit/word module.

In operation the clock decoder in Figure 2 will supply clock pulses during any cycle in which the chip is selected (Figure 3 – cycle 1 and cycle 6) or when the memory is being refreshed (Figure 3 – cycle 4) and will supply an extra Phase 1 pulse on the first cycle after deselecting the chip (Figure 3 – cycle 2). During all remaining cycles the chip is deselected and no clock pulses are supplied to the chips.

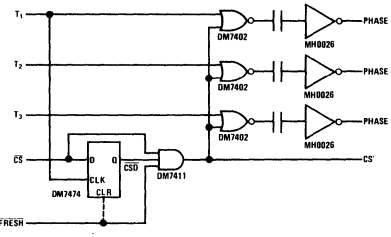

FIGURE 2. MM5262 Clock Decoding Logic

There are three practical considerations to be aware of when using this circuit. First is that, although the power supplies need only be large enough to supply the average current to the memory and its clock drivers, the capacitance bypassing the power supplies should be large enough to supply the peak current during refresh without excessive power supply droop. The second consideration is that if T1 goes to the low state prior to CS or $\overline{\text{REFRESH}}$ going low, the leading edge of Phase 1 will be delayed according to the delay in chip select and T1 pulse width may have to be increased to ensure that the minimum Phase 1 pulse width is supplied to the chip. The third is that if $\overline{\text{REFRESH}}$ goes high after T1 goes low a glitch will be produced on Phase 1. If $\overline{\text{REFRESH}}$ is connected to the clear input of

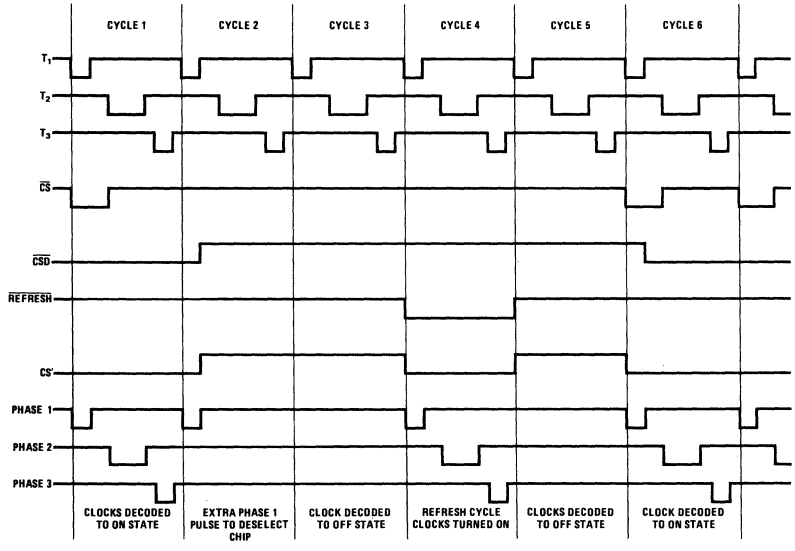

FIGURE 3. MM5262 Clock Decoding Timing Diagram

the DM7474, as shown by the dotted line in Figure 2, the glitch will be extended into a full Phase 1 pulse.

The extra Phase 1 pulse after a refresh cycle will not cause any problems but it will change the value of the refresh current. If refresh is implemented by doing one refresh cycle every 62.4μs, the refresh power will be doubled over what it would be if 32 refresh cycles are done consecutively every 2.0 ms. This is due to the fact that with 32 consecutive refresh cycles the memory receives 33 Phase 1 clocks and with a refresh cycle every 62.4μs the memory receives 64 Phase 1 clocks.

One advantage of connecting $\overline{\text{REFRESH}}$ to the clear input of the DM7474 is that $\overline{\text{REFRESH}}$ is no longer required to be applied for the entire cycle and may return to a one after the positive edge of T1.

It is perhaps of more interest to examine an actual system to determine the effects of clock decoding. As an example a complete 8k-by-16-bit memory has been designed and is shown in Figure 4. This system is not optimized but will serve as a good comparative example. Table II shows power consumption for operating and standby modes with clock decoding and Table III gives power consumption without clock decoding. A comparison between these tables shows a 42% decrease in power consumption by employing clock decoding. Table IV shows various memories mechanized using the basic 8k-by-16 module. Power consumption is given with and without clock decoding for cycle times of 635 ns and 1,000 ns. It is clear from these tables that as memory size increases clock decoding becomes essential. Saying this another way, the ratio of a memory components operating power to standby power is an important parameter for the designer.

TABLE II. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and Clock Decoding)

	I_{CC} (mA) @ 5.25V		I_{DD} (mA) @ −16V		I_{BB} (mA) @ 8.75V	
	OPERATING	STANDBY	OPERATING	STANDBY	OPERATING	STANDBY
TTL	1,180	1,180	0	0	0	0
MH0026	124	1.2	111	1.1	0	0
MM5262	699	12.8	650	19.2	8.0	6.5
Total Current	2,003	1,194	761	20.3	8.0	6.5
Total Power (Watts)	10.5	6.3	12.2	0.33	0.07	0.057

Total Operating Power = 10.5 + 12.2 + 0.07 ≅ 22.8 Watts
Total Standby Power = 6.3 + 0.33 + 0.057 = 6.7 Watts

TABLE III. Power Consumption of 8k x 16 Module (With t_{CYCLE} = 635 ns and No Clock Decoding)

	I_{CC} (mA) @ 5.25V	I_{DD} (mA) @ −16V	I_{BB} (mA) @ 8.75V
	OPERATING	OPERATING	OPERATING
TTL	1,180	0	0
MH0026	241	231	0
MM5262	1,333	1,290	9.6
Total Current	2,754	1,521	9.6
Total Power (Watts)	14.4	24.4	0.875

Total Operating Power = 14.4 + 24.4 + 0.875 ≅ 39.3 Watts

TABLE IV. Power Consumption of Larger Memory Systems Using Multiple 8k x 16 Modules

MEMORY SIZE	NUMBER OF CARDS	TOTAL POWER (Watts) t_{CYCLE} = 635 ns		TOTAL POWER (Watts) t_{CYCLE} = 1,000 ns	
		CLOCK DECODING	NO CLOCK DECODING	CLOCK DECODING	NO CLOCK DECODING
8k x 16	1	22.8	39.3	16.9	25.8
8k x 32	2	45.6	78.6	33.8	51.6
16k x 16	2	29.5	78.6	23.5	51.6
16k x 32	4	59	157.2	47	103.2
32k x 16	4	42.9	157.2	36.7	103.2
32k x 32	8	85.8	314.4	73.4	206.4

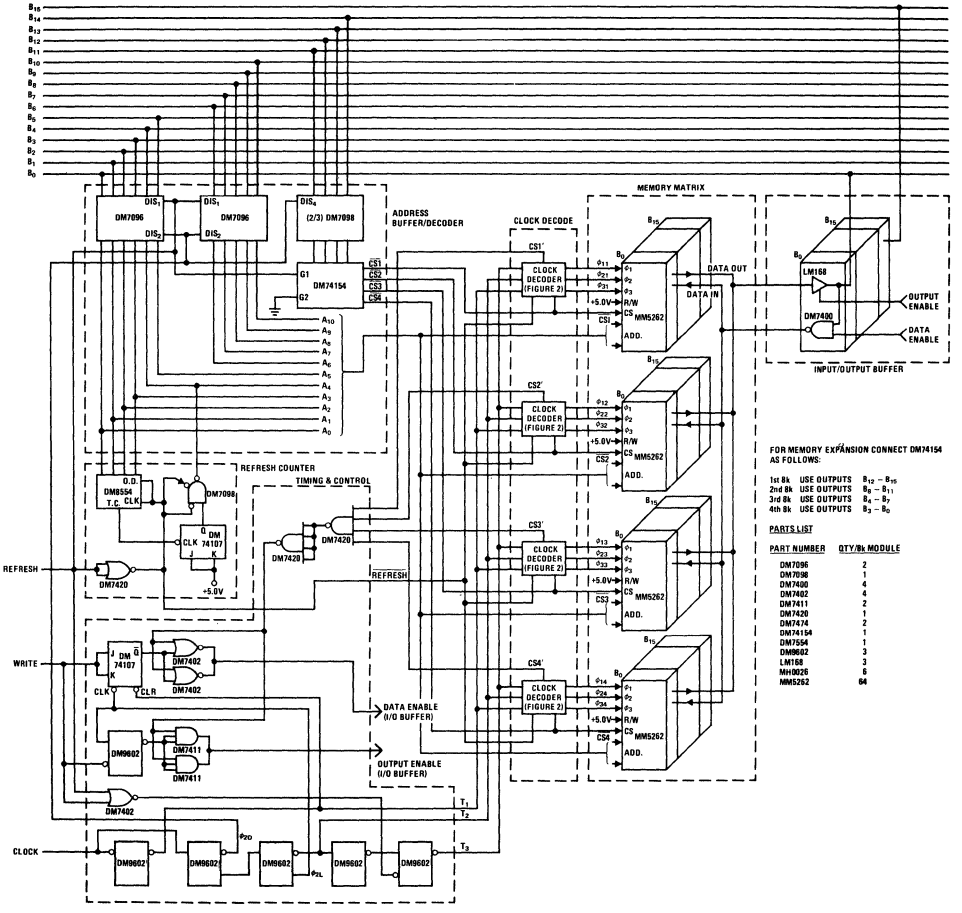

FIGURE 4. 8k x 16 Memory Module