LOW FREQUENCY OPERATION WITH DYNAMIC SHIFT REGISTERS

In many dynamic shift register applications, it is advantageous to operate the circuit at low clock frequencies or in clock burst modes where high frequency clock rate periods are followed by long intervals in which the clocks are absent. To insure that his system will operate correctly under these conditions, the designer should be aware of the limitations of the type of shift register he is using.

There are two basic forms of dynamic shift register cells: the ratioless and the ratio. The ratioless circuit of Figure 1a is based on a capacitor precharge concept. During ϕ_{IN} clock time, node B is precharged by transistor Q_3; i.e., Q_3 is turned on by ϕ_{IN}, creating a low impedance path from node B to V_{GG} which charges the node capacitor C_2 to a negative voltage. Data is coupled at the same time through transfer transistor Q_1 to node A, the gate of Q_2. If the incoming data is a positive or "0" level, Q_2 will be in a high impedance off state, and node B will charge to a negative voltage one threshold more positive than the ϕ_{IN} clock amplitude.

When ϕ_{IN} returns to a positive level. Q_3 is shut off, isolating the precharged voltage of node B. The stored charge of node B, coupled with an additional increment contributed by C_4, redistributes between nodes B and C when the ϕ_{OUT} clock turns on transistor Q_4. The redistributed charge develops a negative voltage "1" level across C_3 which becomes isolated when ϕ_{OUT} returns to a "0" level. The "1" level turns on Q_5, resulting in a low impedance path between the output of the cell and V_{SS}, establishing a "0" level at the output.

In the ratioless cell, there are two nodes which become isolated from any charge replenishing source during normal operation of the circuit: nodes B and C. These are the nodes which establish the low frequency limitations of the cell. In most designs node C, the gate of the logic transistor Q_5, is the limiting node because total capacitance is less. If we had assumed the initial data coupled by Q_1 during ϕ_{IN} to be a "1" level, then node A would of course be the limiting node of the cell.

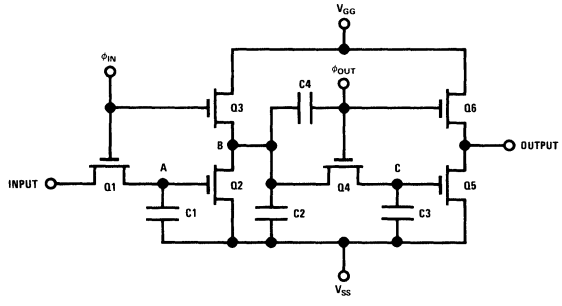

FIGURE 1a. Ratioless Dynamic Shift Register Cell

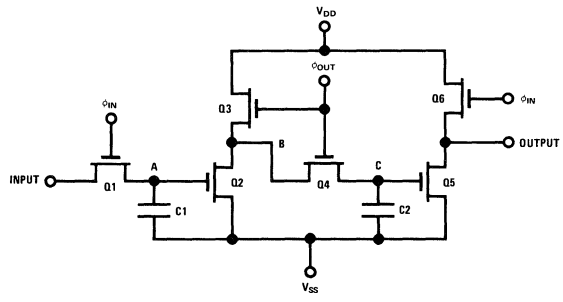

FIGURE 1b. Ratio Type Dynamic Shift Register Cell

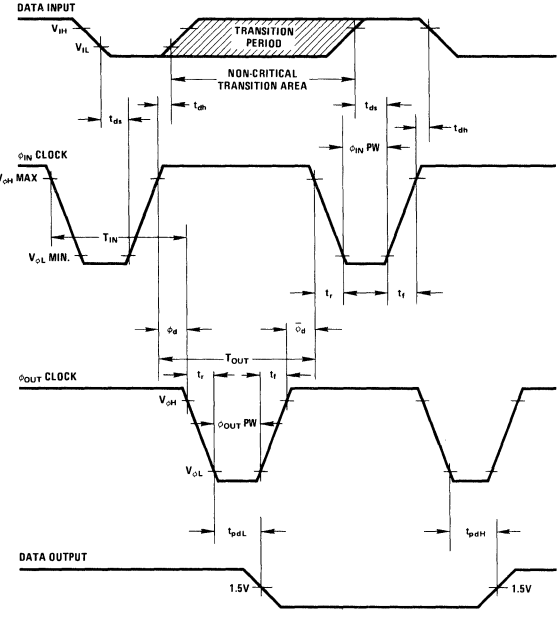

FIGURE 2. Timing Diagram For Two Phase Dynamic Shift Registers

The ratio dynamic shift register cell of Figure 1b has only one isolated node which limits minimum frequency operation. It, like the ratioless cell, is the gate node of the logic transistor. The ratio cell does not rely on stored precharge to establish a "1" level on a succeeding logic gate mode. If a "0" level had been transferred to node A of the ratio cell by Q_1 during ϕ_{IN} time, Q_2 would be off. A ϕ_{OUT} "1" level would turn on Q_3 and Q_4 creating a charging path between node C and V_{DD}, resulting in a "1" level at node C. The node would be isolated by Q_4, just as in the ratioless cell, when ϕ_{OUT} returns to a "0" level.

If the data coupled by Q_1 had been a "1", both Q_2 and Q_3 would be on during ϕ_{OUT} time. To establish a "0" at node B in that case, an electrical ratio between the on impedance of Q_2 and Q_3 must be considered by the cell designer.

Charge must be stored at the logic transistor gate node of the ratioless cell for the period of time between leading edges of the two phase clocks. This is because no charge enters the node B and C network after the leading edge of the transfer clock (ϕ_{OUT}) and there is no way for charge which leaks off the nodes to be replaced. This portion of the clock period is defined as a Partial Bit Time. The Partial Bit Time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is the T_{IN} period, and the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is T_{OUT} (Figure 2).

The period of the minimum operating frequency is the sum of the two, or

$$\phi_f\,(\text{MIN}) = \frac{1}{T_{IN} + T_{OUT}} \qquad (1)$$

Obviously the lowest operating frequency can be attained when T_{IN} and T_{OUT} are each at their maximum limit and therefore equal. This says that for minimum frequency, 50% clock phasing should be used, i.e., the clocks should be equally spaced within the bit time.

The ratio cell has a similar storage requirement, but with one difference. During the time the transfer clock (ϕ_{OUT} in Figure 1b) is on, a source of charge is available to node C through the ON transistors Q_3 and Q_4, assuming Q_2 is OFF. Therefore, charge must be stored on the critical capacitor C_2 only after the transfer clock has returned to a "0" level, and isolated the node. This required storage time is usually referred to as Clock Phase Delay Time (ϕ_d). The phase delay time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is ϕ_d; the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is $\overline{\phi}_d$ (Figure 2). Minimum clock operating frequency is:

$$\phi_f\,(\text{MIN}) = \frac{1}{\phi_{IN}\,PW + \phi_d + \phi_{OUT}\,PW + \overline{\phi}_d} \qquad (2)$$

assuming clock rise and fall time $\ll \phi_{PW}$.

Optimum low frequency operation can be obtained when the clock pulsewidths and phase delays are maximized and made equal. In most cases this would mean 10 μs clock pulsewidths and 50% clock phasing. For power or system application reasons it is usually not convenient to use such wide pulsewidths, and the minimum clock frequency is simplified to

$$\phi_f\,(\text{MIN}) \cong \frac{1}{\phi_d + \overline{\phi}_d} \qquad (3)$$

assuming $\phi_{PW} \ll \phi_d$ or $\overline{\phi}_d$.

Maximum Partial Bit Times and Clock Phase Delays for a given circuit are a measure of the ability of the critical nodes within the cell to store a minimum voltage level. Charge is usually lost due to leakage currents associated with the semiconductor junctions of the nodes. The total reverse leakage current for a p-n junction is the sum of three components; the bulk diffusion current, charge generation current and surface leakage current. Within the normal operating junction temperature range of MOS shift registers (−55°C to 150°C), the charge generation current is the primary component of leakage. Charge generation is usually attributed to recombination centers within the depletion layer of the junction. Leakage current generated in this manner is usually approximated by the expression

$$I_L = KT^{3/2}\,\epsilon^{-7020/T} \qquad (4)$$

Where T = Junction temperature, °K

K = Proportionality constant

I_L = Leakage current of P-N junction

Therefore Partial Bit Times and Clock Phase Delays will be a definite function of temperature. Figure 3 shows a curve for Partial Bit Times as a function of temperature for a typical shift register using a ratio-less cell. Figure 4 gives the corresponding minimum operating frequency versus temperature for two cases: when $T_{IN} = T_{OUT}$ (50% clock phasing), and when one of the Partial Bit Times is minimized, the other maximized. Minimum Partial Bit Time is:

$$T_{(MIN)} = \phi\,PW_{(MIN)} + \phi_{tr} + \phi_{tf} + \phi_{d(MIN)} \qquad (5)$$

Any Partial Bit Time between minimum and maximum at a given temperature can be used. The minimum clock rate would be calculated using Equation 1.

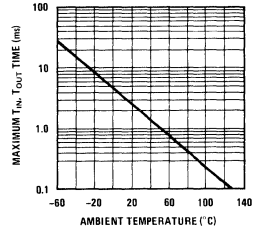

FIGURE 3. Maximum Partial Bit Time vs Ambient Temperature

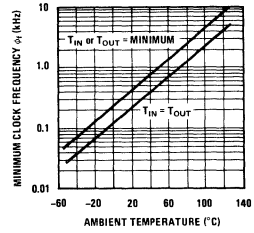

FIGURE 4. Minimum Clock Frequency vs Ambient Temperature

If the shift register utilizes a ratio cell, a curve identical to Figure 3 could be used to obtain maximum Clock Phase Delays for any required temperature. Equation 2 or Equation 3 could then be used to calculate minimum clock frequency at that temperature.

The shift register user can often increase his margin of safety when operating at low frequency, or for long periods of time with the clocks stopped, by designing the system with that operation in mind. The ambient operating temperature of the registers should always be minimized. The cell requires a minimum voltage at the critical node to operate, and the time to discharge the node to that value is dependent upon the initial voltage, as well as capacitance and leakage:

$$t_d \approx \frac{C_{NODE}\,(V_{INITIAL} - V_{MIN})}{I_L} \qquad (6)$$

t_d = T_{IN} or T_{OUT} for ratioless cells;

= ϕ_d or $\overline{\phi}_d$ for ratio cells

C_{NODE} = Total capacitance at critical node

$V_{INITIAL}$ = Voltage at critical node immediately after isolation of that node by transfer clock.

V_{MIN} = Minimum voltage required at critical node for operation.

I_L = Total leakage current at critical node.

The initial voltage can be optimized in two ways: by using the highest clock amplitude possible and by allowing something greater than minimum clock pulsewidth to insure that the maximum amount of charge is coupled to the node (and in the case of the ratioless cell, that the maximum precharge voltage is obtained before transfer). A high value of V_{GG} or V_{DD}, the negative supply voltage, increases on-chip power and therefore junction temperature, as well as increasing the minimum required node voltage. It is a good idea, therefore, to stay away from very high supply voltages. When both the clock driver reference voltage and V_{GG} or V_{DD} are the same supply, the best tradeoff is toward the higher end of the specified range, however. One other consideration which applies during operation at any frequency, but particularly at low frequency, is excursions of the clock line more positive than V_{SS}. This forward biases internal junctions which results in parasitic PNP transistors. If the collector of the parasitic PNP happens to be a critical node, the circuit will fail. Because critical nodes are often closer to the minimum required voltage during low frequency operation, registers are usually more sensitive to positive clock spikes.

When calculating temperature effects of a system operating in the clock burst mode, the designer must remember that power dissipation in the shift register is approximately double at 2.5 MHz what it is at 100 kHz. High frequency bursts will heat the chip, causing high junction temperatures which reduce the time the clocks can be off.

SUMMARY

Dynamic shift registers can be operated at very low clock rates if manufacturers data sheets are consulted and the proper clock phasing is used. Added margin can be designed into systems by keeping clock amplitudes high, the clock pulsewidths 10 to 20% wider than specified minimums, power supplies low and temperatures as low as possible. Beware of circuit board hot spots which increase the temperature of individual packages, or extensive interlead coupling or ringing which could result in positive clock spikes.