



## THE SYSTEMS APPROACH TO CHARACTER GENERATORS

A huge new market for man/machine interfaces is being created by the increasing availability of low cost data processing through computer time sharing, LSI calculators, minicomputers and digital business and control systems. In turn, the pressure is on to design CRT terminals, displays and teleprinters that are at least as compact and inexpensive as the new data processors.

MOS integrated circuit producers are in the thick of this competition. They have begun making read only memories and shift registers with enough storage capacity to put an appreciable dent in terminal and printer costs. Entire alphanumeric character fonts and CRT refresh channels now can be fabricated as single-chip arrays. Low threshold MOS processes and designs have been refined to make the storage arrays more compatible with bipolar logic and standard power supplies.

These developments have won MOS a place on the alphanumeric side of the readout family tree in Figure 1 (and some inroads are being made on the other side—see Appendix in this App. Note. In fact, MOS has pushed beyond the state of the art. MOS/TTL assemblies can generate characters faster than they can be handled by moderately priced CRT video circuitry or printer mechanisms. However, the increased storage capacity and speed also make higher performance systems feasible. For example, designers are considering larger fonts that make characters more legible. Large fonts have generally been economically impractical in the past because even a small increase in font size can double the memory size needed.

## MOS ROMS AND REGISTERS

Large capacity, high speed, and bipolar compatibility strike directly at the problems involved in lowering data terminal costs. To generate and update readouts with many characters and symbols takes thousands of bits of storage and fast manipulation of data and control signals. If this capability is supplied in a central processor, it must be paid for in the form of central system overhead and communications costs. Using pre-LSI memory techniques in the terminals, however, can easily double the cost of each console.<sup>1</sup>

Storage capacities per MOS chip have increased at least tenfold in the past few years, with comparable reductions in assembly costs. By the close of 1969, MOS/TTL character generators cost about half as much as those built with bipolar devices. The newest ROMs (read only memories) for character generation represent the integration of some 3,000 diodes and 50 packages of IC gates. One terminal manufacturer who made the changeover late in 1969 replaced six large printed circuit boards with one plug-in card.

The largest MOS ROMs mass produced last year stored 1024 and 2048 bits—general purpose sizes used for table lookup, microprogramming and random-logic functions as well as character generation. A typical generator contained three 1024-bit ROMs, such as National Semiconductor's SK0001 and SK0002 kits (see Table 1 and Figures 2 and 3). Generating the standard 64 ASCII-selected characters in a 5 x 7 font requires a storage capac-

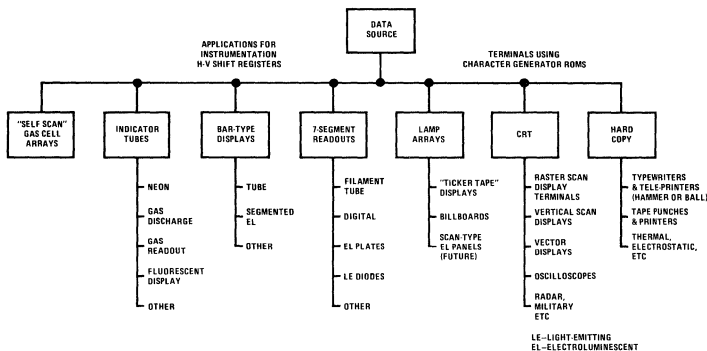


Figure 1. Display Family Tree

ity of at least 5 x 7 x 64. Each logical "1" bit stored in the ROM produces a black dot on a printout or a bright spot on a CRT screen, and each "0" bit a blank space.

Table 1. ROM Combinations for Various Fonts

FONT	CHARACTERISTICS	PARTS REQUIRED
5 x 7	Raster Scan	SK0001 or MM5240
7 x 5	Vertical Scan static ROM required	SK0002 or MM5241
7 x 9	Raster Scan	MM5241 (2 required)
9 x 7	Vertical Scan static ROM required	MM5240 (2 required)
8 x 10	Raster Scan	MM5241 (2 required)
10 x 8	Vertical Scan static ROM required	MM5240 (2 required)
9 x 11	Raster Scan	MM5240 (3 required)
11 x 9	Vertical Scan static ROM required	MM5241 (3 required)
12 x 16	Raster Scan	MM523 (6 required)
16 x 12	Vertical Scan static ROM required	MM5241 (4 required)

Two new soon-to-be-announced ROMs are the MM5240, storing 64 x 8 x 5 bits, and the MM5241 storing 64 x 6 x 8 bits. Each chip also contains decoding logic and sense amplifiers (as do the 1024 and 2048-bit chips). Thus, one ROM is ample for a standard 5 x 7 or 7 x 5 font. The added capacity can implement special needs, such as dropping comma tails below the other characters and symbols. But its main purpose is in providing the logic and programming flexibility that enables ROMs to be operated in tandem to generate the larger font sizes indicated in Table 1. The additional capacity costs little in terms of silicon real estate because these devices are made by low-threshold processes with p-channel-enhancement mode MOSFETs as the storage elements—the most LSI-able type of MOS.

In the past, when diode matrixes were used as character generators, the 5 x 7 or 7 x 5 fonts gave the best cost/legibility tradeoff. Because the new ROMs lower the cost per function, the 8 x 10 font will probably become the most attractive.

The input-output configurations of the MM5240 and MM5241 are outlined in Figure 4 for a standard ASCII-addressed font. The 6-bit ASCII code words will address any of 64 characters ( $2^6$ ). The control logic generates the three additional address

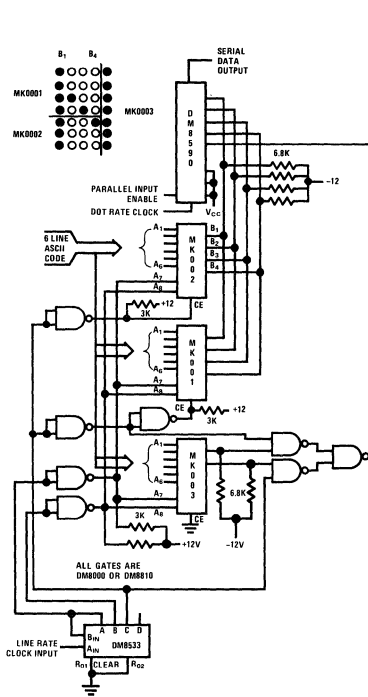


Figure 2a. Three-ROM Raster Scan Character Generators

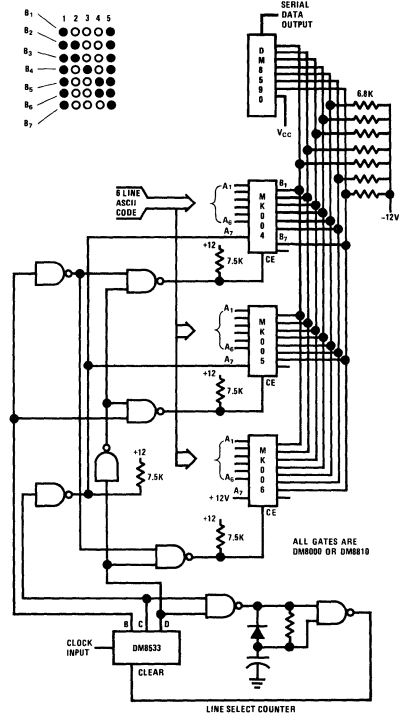


Figure 2b. Character Generator For Tape Printers and Other Vertical Scan Applications

CHARACTER SELECT															
I <sub>1</sub>	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
I <sub>2</sub>	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
I <sub>3</sub>	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
I <sub>4</sub>	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7

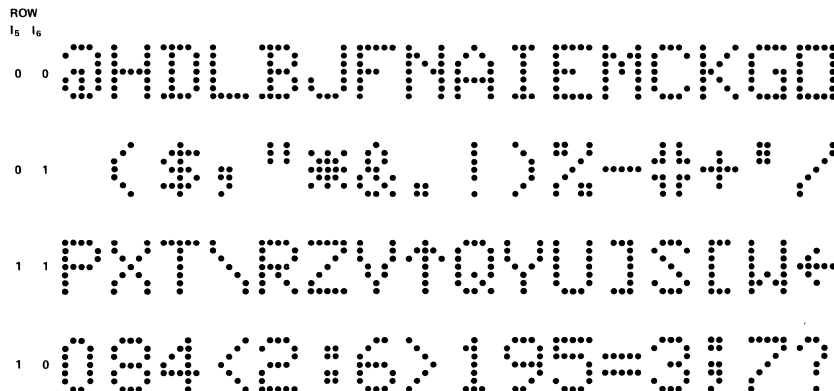


Figure 3a. Raster Scan Character Font

CHARACTER SELECT															
I <sub>6</sub>	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
I <sub>5</sub>	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
I <sub>4</sub>	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
I <sub>3</sub>	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7

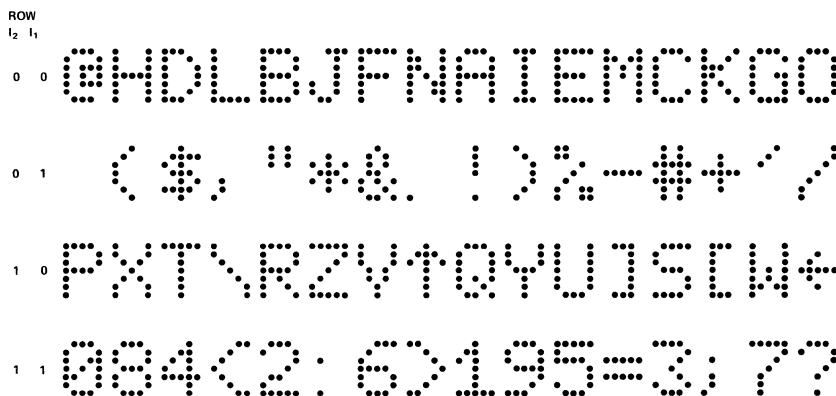


Figure 3b. Vertical Scan Character Font

bits needed to select the individual lines or columns of dots that form the characters in the

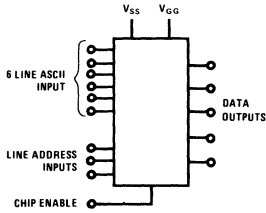


Figure 4a. MM5240 Raster Scan Character Generator Element

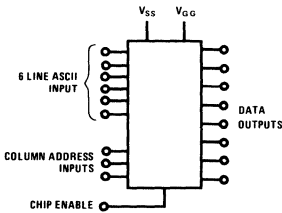


Figure 4b. MM5241 Vertical Scan Character Generator Element

5 x 7 x 64 dot matrix. The output bits forming each dot line or column are presented in parallel. The parallel outputs are serialized by a TTL register and used to control the CRT beam or the printer mechanism. To simplify the selection process, the ROMs are programmed to generate the lines or columns in the correct sequence when addressed by the sequential outputs of a TTL counter.

As for registers, they became quite popular during 1969 because a CRT refresh memory of up to about 5,000 bits—enough for a display of more than 800 characters—could be built less expensively with MOS dynamic registers than with delay lines.<sup>2</sup> This was achieved with registers containing 200 storage stages per chip. During 1970, dynamic registers up to 512 bits long will go into mass production, giving rise to predictions of significant savings in refresh memory costs. Whether savings that large can actually be realized will depend upon how quickly the new devices catch on and go into volume production.

Aside from cost per function, other pertinent consideration are temperature sensitivity and functional flexibility. In a refresh memory, register outputs are fed back to the inputs. On each recirculation, the data readdresses the ROM, regenerating (refreshing) the display (Figure 5). The recirculation times must correspond to the CRT scanning time to keep the display legible. MOS register delay times are relatively insensitive to temperature variations because they are established by system clock rates rather than physical parameters.

Also, special requirements of data entry and output for display formatting and editing can be implemented much more easily with registers than with physical delay lines. Data bit positions in the recirculation loops are maintained in alignment and can be monitored and modulated precisely by the control logic (one recirculation loop is needed for each data bit—six loops, for example, in an ASCII-addressed system). Data entry and output for display or transmission thus becomes a straightforward exercise in logic design.

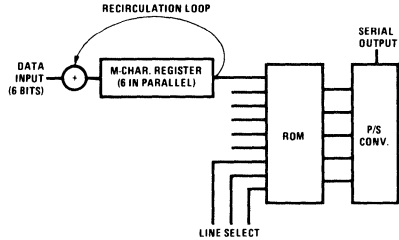


Figure 5. Basic Digital Character Generator and CRT Refresh Memory

### BIPOLAR COMPATIBILITY

A dynamic register is one that must be clocked at some minimum frequency. Data is retained in the form of charge storage and the charges would eventually leak out of the storage nodes if not re-established. In contrast, the ROMs being discussed are static devices, generating an output only when addressed. Specifically, they are designed and programmed to be sequenced by TTL ICs. Furthermore, the new generations of ROMs and registers accept and put out bipolar level signals and operate off +5 volt and -12 volt power supplies.

These features eliminate any need for special level-translating circuits between the MOS and bipolar devices. Also, special power supplies are not generally required because ±12V as well as ±5V supplies are usually provided in terminals for other parts of the system. Such compatibility is a convenience and a cost saver in any digital system containing MOS storage subsystems and bipolar logic, since it minimizes the interface and drive complexity. In terminals, though, compatibility is practically essential for efficient operation and lowest cost per function.

First, as the detailed system diagrams show, many of the interconnections have a MOS device at one end and a TTL device at the other, so that a large number of level translators would be needed if they were not compatible.

Second, several control logic operations must occur between memory outputs, and the output-serializing device must operate at least six or eight times as fast as the word (dot line or column) output rate of the ROM. Obviously, if high speed

control logic—preferably TTL MSI devices such as single-chip binary counters and 8-bit parallel-input/serial-output shift registers—were not used, the character generating process would be slowed excessively. This would limit the number of characters that could be displayed in a CRT refresh cycle or printed out in a given time. The new generation of MOS ROMs can deliver up to eight bits in parallel in about 700 nanoseconds, compared with a microsecond or more for last year's models. Logic speeds around 10 MHz are therefore desirable (several times higher than the speed that can be achieved by MOS gates.) Likewise, dynamic registers can now easily be run at rates above 2 MHz—double the speed of early mass produced registers—so the logic controlling refresh storages must also be faster.

The improved compatibility and higher speed are largely due to better design and processing of the input and output stages of the registers and the sense amplifiers of the ROMs. They don't increase the complexity of the MOS circuitry, unlike other techniques for increasing MOS speed, and therefore they have permitted the capacity increases cited.

The net benefit to the system designer of this approach to MOS design is that it enables the system designer to capitalize on the best features of each technology—MOS storage for high density and low cost, and TTL for high speed processing of data and control signals. This is what produces lowest cost per function in most digital systems.

**CRT RASTER SCAN DISPLAYS**

The basic refresh mode in Figure 5 limits the number of characters that can be displayed. A better way of generating and refreshing raster scan displays, particularly those with many rows or lines of characters, is outlined in Figure 6. Figure 7 illustrates the timing and logical implementation for a multiple row system.

As before, coded data from a communications link or the console keyboard passes through the registers and addresses the character generator. In these examples, the 6-bit ASCII input and the 3-bit control logic input generate raster scan character formats that allow a conventional TV monitor to be used as a display. Communications codes other than ASCII can be used.

If the ROM contains a 5 x 7 font, each 5-bit character line output will form five horizontal bright spots on the CRT. That is, each ROM output generates one-seventh of each character in a row of displayed characters. The output is serialized by the TTL register and used to intensity modulate the CRT beam as it sweeps across the screen.

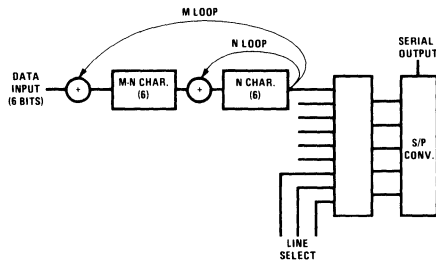
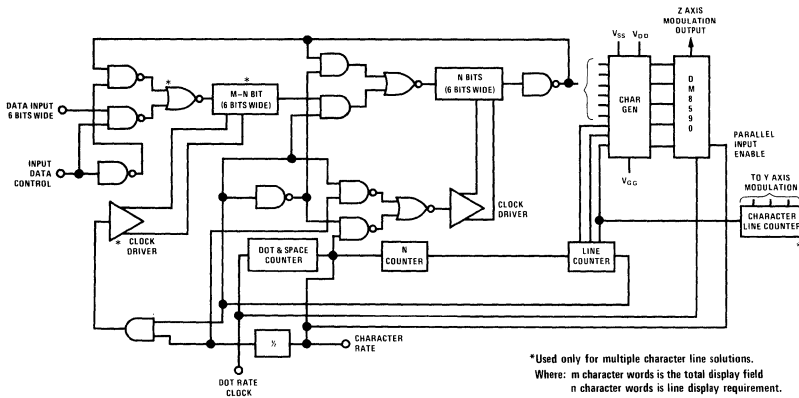


Figure 6. (M-N)+N Technique for Large Page Displays

The refresh memory registers are divided into M-N and N sections to facilitate page displays. M is the total number of characters displayed in several rows (lines of the page) and N is the number of characters in each row. To form such a display with single-loop registers, as in Figure 5, would take seven recirculations of all M data words during each refresh cycle of the CRT. The technique in Figures 6 and 7 only requires high speed recirculation of N bits at a time, with advantages that will be discussed shortly.



\*Used only for multiple character line solutions.  
Where: m character words is the total display field  
n character words is line display requirement.

Figure 7. Multiple Row Raster Scan Display System

Assume that on the first sweep of the CRT beam, the ROM is being addressed by the six register outputs representing characters  $N_1$ ,  $N_2$ ,  $N_3$ , etc. The first horizontal, 5-dot line of each character in the display row are displayed in sequence. Then the line address inputs to the ROM from the control logic change to their second state at the time that  $N_1$  has completed its recirculation to the N register's outputs. Thus, on the second CRT sweep, the second series of 5-dot lines are displayed horizontally for all N characters. At the end of seven recirculations, the complete row of N characters is on the display.

Now, the contents of the N register are not returned to the input of the N register. Instead, they are fed back to the input of the M-N register and this register is clocked to load the N register with the second group of N characters. The M-N register is then held still while the N register recirculates seven times to generate the second row of characters on the display. After all M characters are on the display, the first group of N characters is reloaded into the N register and the entire process is repeated to refresh the display.

Human factors—chiefly the eye's response time—dictate that the display be refreshed at least 30 to 35 times a second for good legibility. Most designers prefer to refresh at 60 Hz power line frequency because it is generally the most convenient frequency.

Besides generating the line address inputs (that is, the number of recirculations of the N register), the control logic keeps track of the number of dots and spaces in the output bit stream. The spaces between characters in a display row are inserted as "0" bits when the ROM outputs are serialized by the TTL register. The counters also control the loading and recirculations of the MOS registers in the refresh memory subsystem.

A multiple row raster scan display could be generated with the M-loop technique in Figure 5 but, the implementation is difficult and impractical. This technique is more appropriate for single row displays. Using this method of display, all M characters to be displayed must recirculate seven times to generate a 5 x 7 horizontal scan, so all stages of the registers must operate at the full character rate. To form several rows with a single-loop memory requires an interlaced scan rather than an ordinary raster scan. The first series of 5-dot lines are generated by the first N character outputs as before, but the next set of N inputs to the ROM will generate the first group of 5-dot lines in the second row of characters on the display. Therefore, the beam must jump to the new line position. To display four rows of 5 x 7 characters, for instance, would require a staircase generator that would step the beam by the height of nine scan lines (seven dot lines, plus two blank spacing lines between rows) three times after the initial scan.

Then, as the second of the seven recirculations begins, the beam would have to be shifted an additional line to start the second series of line scans—and so forth.

The M-N-N technique does not require any more register stages than the M-loop technique and significantly reduces control and drive circuit requirements—again producing a lower cost per function.

### REFRESH MEMORY MODULATION

The technique employed in the M-N refresh memory is called "clock modulation". In other applications, it has already been found to significantly reduce total storage costs.<sup>3</sup> It helps minimize power dissipation—in most terminals, the amount of power consumed is unimportant in itself since line power is used, but registers are powered by clock drivers and the cost and complexity of the drive network is certainly important. Furthermore, the technique allows long, very high-density MOS circuits, produced by relatively inexpensive low threshold (bipolar compatible) processes to operate at very high effective character rates.

As shown in Figure 7, the raster scan system uses nine clock intervals to generate a row of characters on the display. Seven are for the high-speed recirculations. During the other two intervals, the first N characters are fed back from the output of the N register to the input of the M-N register while the N register is loaded from the M-N register with a new row's worth of characters. Since two intervals are used for this operation, the registers operate at only half the character rate. The rest of the time, the M-N register is charge-quiescent. Its average clock frequency is only about 11% of the character rate.

In other words, most of the refresh memory (perhaps 90% in a large display system) operates at only half the character rate (say 1 MHz instead of 2 MHz) only two-ninths of the time. The savings in the drive network alone can be judged from the power-frequency plot for a typical MOS dynamic register (Figure 8)<sup>3</sup>. In addition, the designer can

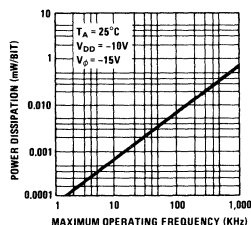


Figure 8. Power vs Frequency Plot of Typical MOS Dynamic Register

increase the number of characters generated per refresh cycle, for a larger display, or increase the number of dot lines, for a larger font, or both.

Remember, though, that dynamic registers must be clocked to retain data. How long can the M-N register be turned off? Long enough for practical applications. The guaranteed minimum frequency is temperature dependent, since temperature affects charge-storage time. The minimum for National Semiconductor's MM-series registers is 500 Hz at 25°C, rising to 3 kHz at 70°C (maximum operating temperature is 125°C, but that is not a display environment). At room temperature, the registers can safely be quiescent for as long as 2 msec. (The typical MM register will actually hold data for 10 msec.) Suppose the N register stores 40 characters and operates at 2 MHz. The quiescent period can be as short as  $40 \times 7 \times 0.5 = 140 \mu\text{s}$ . If standard TV raster timing is maintained then the quiescent period will be  $7 \times 63 \mu\text{s} = 441 \mu\text{s}$ . Obviously, the designer has great leeway in character rates, operating temperatures, and register capacities.

Other applications in displays for clock modulation include input-output buffering of data during data reception and transmission,<sup>2</sup> or during display editing and formatting through the console keyboard. The register rates can be adjusted via control logic to accommodate differences between I/O and recirculation rates. Note that the gating in Figure 7 permits data entry under TTL control into either register section.

### CHARACTER GENERATION

The first generally available MOS character generators were kits such as those in Figure 2, using three 1024-bit ROMs (MM521). Although single-chip generators were being developed in 1969, they were in very short supply. The kits cost about half as much as diode generators and thus allowed terminal manufacturers to start the changeover to MOS.

The kits are also a good place to begin describing character generator operation in this application note, because they provide an "exploded view" of multi-ROM generator operation. Similar techniques will be needed to build larger fonts with the new devices. The external gating functions shown in Figure 2 are not needed for these fonts when the MM5240 and MM5241 are used. The "assembly" of the dot patterns is taken care of in the programming of the ROMs. However, to generate a large font, such as  $8 \times 10$  or  $12 \times 16$ , with the new ROMs will require operation of two to four ROMs.

Each MM521 in the SK0001 raster scan kit can store 256 4-bit dot patterns. As the inset letter "N" in Figure 2a indicates, the MK001 ROM stores the first four 4-dot line segments of each of the  $5 \times 7$  characters, the MK002 stores 4-bit segments of the other three-dot lines, and MK003 supplies the fifth bit of each of the seven-dot lines. All ROMs are addressed simultaneously.

The 6-bit ASCII code was devised to select 64 ( $2^6$ ) characters. However, an 8-bit address is used to

select the dot lines and the 6-bit ASCII code from the 256 ( $2^8$ ) word locations in each ROM. These two additional bits are supplied by the A and B outputs of a TTL binary counter DM8533 (SN7493) and the counter's C output is used to commutate the MK001 and MK002. The ROMs are enabled by an output at the TTL logical "0" level. Thus, with the gating shown, the MK001 is enabled during the first four of seven line-rate clock inputs and the MK002 during the remaining three inputs.

The MK003 is continuously enabled by grounding the chip-enabled pin, CE. It must generate a 1-bit output for each of the  $7 \times 64$  dot lines in the 64-character set, which implies a 9-bit address. Rather than produce a special ROM just for this function—which would make it expensive—the MM521 was programmed to generate 256 2-bit outputs from the 8-bit address. The counter's C output simply gates out the unwanted bit.

For a  $5 \times 7$  font, the new single-chip character generators are simply programmed to generate all 5 bits in each dot line, from a 9-bit address. Standard programming provides the 64-character ASCII set, but special characters can be substituted by changing the stored dot patterns. The reprogramming process consists of altering an etching mask that controls gate insulation thickness in the MOS field effect transistors of the storage array. If the oxide is left thick, the transistor will not switch when selected by the decoding logic, generating a "0" output from that location.

Figure 9 indicates why the storage capacity of the MM5240 is  $5 \times 8 \times 64$  rather than  $5 \times 7 \times 64$ —each ROM can generate half of the  $8 \times 10 \times 64$  character set. The ROMs can be addressed simultaneously, as before, and be commutated by the

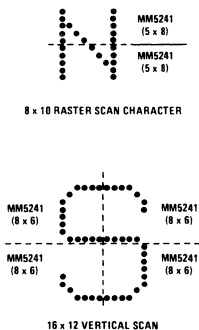


Figure 9. Multiple ROM Character Fonts

control logic to put out the 8-dot horizontal lines in the correct sequence. For very high speed character generation, the addressing of the ROMs can be skewed or overlapped so that the outputs from one are generated while the inputs to the other are being decoded. The only real limitations to the

character generation rates achievable with such techniques are the speed of the bit serializing logic and the bandwidth of the video circuitry.

**CONTROL LOGIC**

Starting with the dot/character or dot and space counter in Figure 7, the counter moduli are set to accomplish the following functions:

- The dot and space counter determines the number of horizontal spacing bits between characters in the character row on the display. Its output is loaded into the parallel inputs of the DM8590 serial-in/parallel-out shift register. For a 5 x 7 font, for example, a modulus of six inserts one spacing bit (logical "0" bit) between each 5-dot group in the serialized stream. During line recirculation periods, this counter also drives the N counter at the character shift rate of the N register.
- The N counter causes the line select counter to change state at the end of every recirculation of the row data in the N register. It generates a pulse at intervals of 6N dot clock periods (assuming one spacing bit).
- The line select counter generates seven sets of the three address bits that sequence dot-line selection from the ROM.
- A character line counter is needed in some raster-scan displays to keep track of which page line has just been generated. This time is signified by the C or D output of the line select counter.

Outputs of the first three counters actuate the register clock drivers, keeping the line select bits in synch with the data code. If the line select counter is a 4-bit binary device, eight states are available on the ABC outputs (000 through 111). The D output can be used to provide a ninth state and the reset function. Only seven states are needed for line select, so the eighth and ninth states provide the interval needed for loading the N register from the M-N register, as previously described.

**VERTICAL SCANNERS AND PRINTERS**

Vertical scan character generators are generally used in hard copy applications. Also, a vertical scan type of character generator can sometimes be more suitable for CRT displays than raster scan.

Displays or printouts of calculators and small business machines often show only numerals and a limited variety of symbols—not enough for a full alphanumeric generator. Such fonts are easily programmed into a small ROM such as the 1024-bit MM522, which stores 128 8-bit words. There's room for 16-5 x 7 dot characters on the chip.

These ROMs are also used in the SK0002 kit for a 64-character ASCII-addressed font (Figures 2b and 3b), which requires the storage of 320 7-dot columns and a 7-bit address. Connected as shown,

the DM8533 TTL binary counter will reset on the count of 16. And with the gating and interconnections shown, the column select cycle is:

Counter Outputs DCB	ROMs Enabled
DCB	
000	MK004
001	MK005
010	MK004
011	MK005
100	MK006
101	reset (instantaneous)

A CRT beam can be intensity modulated by the serialized output, as in the raster scan technique. However, the electron beam traces either a sawtooth or pedestal-type scan pattern on the screen (Figure 10). Every column of each character in the display line is scanned in sequence, starting at the left-hand side of the screen.

The sawtooth scan is straightforward, but the pedestal scan requires that the bit order be reversed in the second and fourth columns. To do this, the outputs of the MK005 ROM are simply connected to the output buses in the reverse order (i.e., output 1 to bus 7, output 2 to bus 6, etc.).

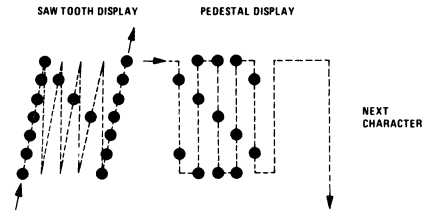


Figure 10a. Two Techniques for Vertical Scan



Figure 10b. Example of Character Generation Using Pedestal-type Scan.

Long shift registers, operating at relatively slow rates can be used. The character rate—the register shift rate—is no more than 1/6 of the column-select rate for a 5 x 7 font, since the beam traces one complete character before going on the next one. A dot counter loads spacing bits between characters via the TTL shift register, a character counter triggers the sawtooth or pedestal scanning patterns, and a row counter would control positioning of the beam in a page display system.



In the new single ROM (MM5241) version of this system, (Figure 11), a 9-bit address is needed, 6 bits for the ASCII code and 3 bits for dot column select. Since the ROM stores five dot columns for each of 64 characters in a 5 x 7 font, 3 decode line are necessary. Also, the ROMs are programmed differently for sawtooth or pedestal scanning. Because the output pins are committed for all columns, external connections cannot simply be used to reverse output bit order.

Hard-copy printers can use the same fonts as vertical scan CRT displays. MOS registers may be used for data input buffering, but of course refresh registers are not generally required. The character generator output may be used to select some combination of 35 hammers, needles or electrodes that print the 5 x 7 dot patterns on the paper. One technique for handling the character generator output is shown in Figure 12.

In Figure 12, a TTL counter connected to divide by six (five columns and the blank column space between characters) generates the column select address. The ROM's outputs are accumulated in TTL latches (or held in TTL serial-in/parallel-out shift registers). When all dots for a character are

ready, they are printed. In tape printing applications in which a 7-transducer array sequentially prints or punches a column at a time as the paper moves under the transducers, the ROM outputs can be used as they are generated unless storage is required for some other purpose.

Character generators are not needed for conventional electromechanical typewriters. But MOS ROMs do have a role here—one version of the MM521, for example, is programmed to convert the ASCII communications code into the Selectric code used to control ball-type printers.

**PRINTING APPLICATIONS**

The application of character generators in a printing application is normally quite different from that of the display system. Most printers require that a total character font be available before the print is executed. An example of a practical method of accomplishing this (Figure 12) is to sequence the character generator element through the font sequence. Each of the character columns or rows is addressed. The character generator output data at each of these address intervals is transferred into bipolar memory. This

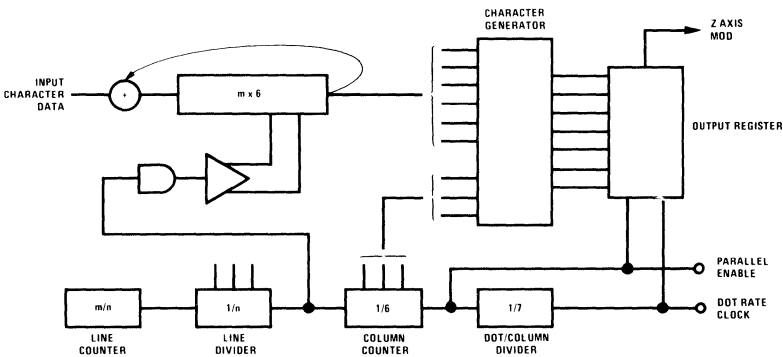


Figure 11. Vertical Scan Display System

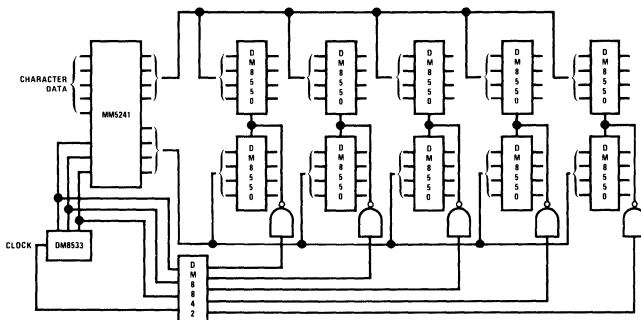


Figure 12. Printer Application Block Diagram

memory not only satisfies the memory storage but also the general power buffer which is required between the MOS character generator and the electromechanical on thermo electric printer. In the printer application there may be a requirement to buffer the input data with data storage because of the relative differences in data and printer rates but generally there is no need to retain the printed character intelligence.

The data transfer from the character generator to the bipolar memory in Figure 12 is accomplished by sequencing the column address lines and enabling the appropriate memory simultaneously. Each pair of DM8550s (SN7475s) then contains the data for one of the five columns in a character. The DM8842 (SN7442)—one in 10 decoder provides the decoding functions which are connected to the enable line on the quad latches.

### LARGER, FASTER SYSTEMS

Most low cost terminal designs have been based on the 5 x 7 font because of the high cost of diode matrixes and wideband video circuits. But it is by no means the most legible font. A 5 x 7 font is acceptable for applications in which the display changes slowly, but human engineering studies indicate that it causes severe eyestrain when an operator reads rapidly changing data.

The greatest portion of the discussion has dealt with a 5 x 7 font. A full 64 character display can be coded into a single MOS package. Now that LSI has entered the scene, we see a different trend towards larger, more stylized font. The economy of MOS ROMs will provide the customer with a more legible character font at the present cost of "discrete" character generators. An analysis of the most practical solutions to various fonts are tabulated in Table 2. The part types which have been used to generate a 64 x 7 x 5 raster scan font are the SK0001-3 ROM kit or the MM5240 which is under development. The vertical scan font is satisfied by the SK0002-3 ROM bit or the MM5241 which is under development. If we examine the other possible fonts, these same two monolithic elements will satisfy the requirements if they were 64 x 8 x 5 and 64 x 6 x 8 respectively. Therefore, the added memory storage is being incorporated into the MM5240 and MM5241. In some of these cases the font is scanned in the horizontal dimension while in others the font is scanned in the vertical dimension. You find both the 8 x 5 and 6 x 8 elements capable of satisfying the font matrix requirement. Since all the ROMs listed are static by design, there are no special clocking hardships induced with the solution of any of these larger fonts. This is not true for all dynamic ROM solutions.

As mentioned before and shown in the table, the same ROM element is used in both raster scan or vertical scan applications. If we recall the design solutions showing the refresh memory and character generator for a 5 x 7 display, the first thing

which is apparent is that the sequencing of the character generator is different in each of the two basic techniques. In one case the character generator is sequenced at the character rate (raster scan) while in the other case the generator element is sequenced at the column rate (vertical scan) of the font.

Since a display utilizing the vertical scan techniques has input address changes at some multiple of the display character rate, a clocking system for a dynamic ROM character generator must be supplied. This requires the addition of a frequency divider and clock generator which results in a higher system cost when dynamic ROMs are used.

A second consideration which should not be overlooked in systems cost is the compatibility of ROMs in multi-package character fonts. Optimum ROM usage and organization will result in lower systems cost. ROMs will also find applications in micro-programming and code conversion where synchronous operation is preferred.

The 8 x 10 font is much better and 12 x 16 is almost optimum for legibility. Small, lower case characters can be sharply defined, too, and they almost appear to be drawn with continuous strokes.

System designers considering these fonts for low-cost displays run, at present, into CRT cost problems. The least expensive displays are television-type CRTs with limited video bandwidth. Bandwidth also limits the number of characters that can be displayed simultaneously. Not counting the times required for beam retrace and functions other than character generation, which reduce the time available in a refresh cycle for dot handling, the necessary bandwidth is roughly:

$$\begin{aligned} \text{BW} &= (\text{dots and spacing bits per character}) \\ &\quad \times (\text{characters per display row or page}) \\ &\quad \times (\text{refresh rate}) \end{aligned}$$

TV-type CRTs have a maximum bandwidth of about 4 MHz, of which only about 2.5 MHz is generally useful. If one uses a 5 x 7 font with one spacing bit (6 x 7 total) at a 60-Hz refresh rate, each displayed character needs 2.52 kHz of bandwidth, so the limit is about 1,000 characters. In contrast, the new ROMs take as little as 700 nanoseconds to generate a dot line, or about 5  $\mu$ s per character. That's fast enough to generate 200,000 characters a second, or a display of more than 3,000 characters at the 60-Hz refresh rate. The actual dot rate in the serial bit stream to the CRT can approach 10 MHz. And if larger fonts are generated in some multiplexed addressing mode, the required bandwidth can be much higher.

Luckily, these problems are not insurmountable and there are alternatives to using oscilloscope-quality CRTs or storage tubes, which are fine for high performance applications but too rich for low cost terminals.

Obviously, the designer can drop the refresh rates. New CRTs with longer persistence phosphors facilitate this. Also, CRT manufacturers have been responding to the new terminal market by working on bandwidth improvements, and they are apparently going to reach 10 MHz in moderately priced video systems soon.

Finally, the designer is not obliged to display his characters digitally just because he uses a MOS ROM. Don't forget that the ROM is really working as a code converter, generating a 35-bit machine language code from a communications code. The language translation can be whatever the situation requires.

All that need be done is update methods used in analog displays, which form characters with strokes rather than dot lines or columns. The ROMs can be programmed such that the bit outputs, when integrated, control X and Y ramp generators. The slopes of the ramp functions are determined by the number of bits in a sequence and the lengths are determined by the locations chosen for turn-off bits. As in the vertical scan technique, the ROM is addressed at the character rate.

Even though some characters can be formed with one or two strokes (I, L, etc.), equal time should be given to all characters in a page display to keep the character rows aligned. A standard sized area of the MOSFET array, such as 6 x 8 or 5 x 8 should be used for each character. Most patterns would thus be a combination of stroke and no-stroke outputs. The single-chip fonts have an 8-stroke capacity for each of 64 characters which is more legible than the standard segmented type of instrument readout, since slant lines could be generated wherever needed.

## APPENDIX

### WHAT ABOUT INSTRUMENTS AND CONTROLS?

While it is safe to predict that 1970 will be "the year of the MOS" in alphanumeric terminals, MOS applications in numeric readouts are just beginning to emerge.

A new device with considerable promise in this field is a high voltage, MOS static shift register, the MM5081. Developed by National, it has a TTL-compatible serial input, 10 parallel outputs that can stand off -55V, 10 latching-type storage stages, and a serial output.

This novel combination of functions means that the MM5081 can drive lamps, numeric indicator tubes, filament tubes in segmented number and symbols displays, electroluminescent panels, and the new gas-cell arrays. In short, it provides MOS with a good foothold on the numeric side of the readout family tree in Figure 1.

The register stages can either shift the bits to the serial output for recirculation or store the data indefinitely. Hence, displayed characters can be swept along a line of indicators, "frozen" on a stationary display, or made to reappear periodically at any desired repetition rate.

A code-converting/character-generating ROM can be placed at the register input, to display numbers and symbols or alphanumerics. A designer can get almost as much flexibility from a lamp or panel display as from a CRT display. In fact, the first application of the MM5081 is controlling a matrix of neon lamps in a moving billboard display.

Some applications for character generators in instruments are also cropping up. Displaying range scales on an oscilloscope is a good idea that can be improved upon with the new ROMs. The display frees the operator of the chores of mentally calculating scale factors and manually writing these on scope photos. With an alphanumeric font, the camera can also record information such as test conditions, date and time of test, identification numbers, etc. Photo sequences and the data needed to analyze the curves can be coordinated automatically.

Similarly, a ROM can be programmed to display standard curves for go-no-go equipment checkout operations. For example, if a radar's pulse amplifier should have certain output characteristics, the ROM generates the correct output curves through a digital-to-analog converter and stroke generator. When an actual operating characteristic and the reference curve are displayed simultaneously, the operator can tell at a glance whether the radar is functioning properly. Many curves or general purpose curve segments can be programmed into a ROM and picked out as needed with selector switches or a ROM microprogrammer.

ROMs can be programmed as lookup tables, random-logic synthesizers,<sup>4</sup> encoders, decoders, and microprogrammers as well as character generators. A single ROM can perform limited combinations of these functions, virtually qualifying it as a microcomputer. It has been suggested that this capability be used in control panels to perform functions like actuating an alarm when a transducer level goes out of range and initiating corrective action. ROM addresses can be derived from digital meter circuitry. In multi-point measuring systems, this would provide the solid state equivalent of a rack of meter relays.

### DEFINITIONS OF DISPLAY TERMS

**Font:** A set of printing or display characters of a particular style and size. A typical dot-character font is 5 x 7, referring to the number of dot locations per character.

**Dot Character:** A character formed by a pattern of bright dots on a CRT screen or dark spots on hard copy, rather than by continuous strokes. The dot

pattern corresponds to bit-storage patterns in a digital memory.

**Column:** In a dot character matrix for vertical scanning, a column is a vertical series of dots. On a page display, a column contains several vertically aligned characters. In this article, a column refers to a dot column.

**Row:** A horizontally aligned group of characters on a display.

**Line:** In this report, line refers to the number of dots displayed in a single scan when a raster scan character is generated. In a 5 x 7 dot character, there are seven lines of 5 dots each.

**Page:** A display consisting of several rows of characters, corresponding to lines on a printed page.

**Raster Scan:** See Figure 9.

**Vertical Scan:** Two types of CRT vertical scans are shown in Figure 10. In hard copy applications, the dots in a column or character may be printed simultaneously by the printing transducers rather than being scanned.

**Sawtooth Scan:** See Figure 10.

**Pedestal Scan:** See Figure 10.

**Dynamic Element:** A digital device that must be clocked. A dynamic shift register must be clocked to retain data. A dynamic ROM is clocked to decode the address and generate an output.

**Static Element:** A device that does not have to be clocked to retain data. A static ROM uses direct coupled decoding for bit selection and static output buffers.

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