Number Cruncher (MM57109) Interface to Microprocessor

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INTRODUCTION

National Semiconductor's number cruncher unit (NCU) is a single chip arithmetic unit (another term for calculator) designed for interface to either a microprocessor driven system or a random logic system. It contains most of the arithmetic functions found in the more complex hand-held calculators and a number of non-arithmetic instructions used in stand-alone system applications. Data transfer is carried out in 4-bit wide BCD digit serial. (Programmable digits number from 1 to 8). Instructions are 6 bits wide. Data format can be selected between floating point and scientific notation mode under program control. Entry is in Reverse Polish Notation (RPN).

The NCU may be powered by either a single supply of 7.9V to 9.5V or a dual supply of 5V and −2.9V to −4.5V. The latter arrangement makes it compatible with some logic devices. The low current drain of 12 mA typical makes it ideal in portable operations. Five internal registers (each 12 digits wide) can be used to store various inputs and results.

The NCU (official part number MM57109) is not entirely custom designed from the ground up, but rather a mask-programmed version of an MOS/LSI chip, the MM5799. The MM5799 is part of a family known as Controller Oriented Processors which includes CPU, ROM, RAM and Input Output on-chip. This group will be discussed more fully in a different section.

FEATURES

- Complex scientific calculator performance
- Entry in Reverse Polish Notation (RPN)
- Digit Entry and Output selectable in floating point or scientific notation
- Selectable mantissa digit count 1 to 8, 2 digit exponents, signs
- Computation in BCD arithmetic
- Handshake in instruction and digit entry
- Alternate high speed synchronous multiple digit entry
- Digit entry and output in 4-bit BCD parallel
- Instruction entry in 6-bit parallel
- Synchronous multiple digit output
- PMOS metal gate low threshold technology
- Internal clock generator driven by single oscillator input
- Low power operation (12 mA typ)
- Control signals to handle input, output
- Automatic power-on initialization at power-up or input provided for external control
- Nonarithmetic instructions performing register manipulation and branch control, etc.
- Microprocessor sense input and flag outputs
- Syntactic and computational error flag

HIGHLIGHTS ON INSTRUCTION SET

The NCU instruction set is designed to interface efficiently to either a random logic system or a microprocessor driven system. In addition to arithmetic functions described below, there are Input Output, Shift, Register manipulation, flag control, jump, and jump on test instructions to help reduce components count to a minimum in a random logic system. Under instruction control, input output data format is selectable between floating point and scientific notation. Input output data length is also programmable between 1 and 8 mantissa digits. There are 3 different methods of inputting and 1 method of output.

There are 64 instructions each 6 bits wide. Instruction execution times range from 1 ms to 1 second. Most are single digit; however, some require the combination of two instructions to perform a complete function. For example: for arc sine; INV, SIN should be executed. Some of the instructions are illustrated below.

0 ~ 9	Digits
.	Decimal Point
EE	Exponent
CS	Change Sign
PI	3.1415927
EN	Enter
ROLL	Internal stack (x, y, z, T) Roll
POP	Stack Pop
+, −, X, /	Plus, minus, multiply, divide
YX	Y^X
SQRT	$\sqrt{X}$
SQ	X^2
1DX	1/X
LN	lnX
LOG	log X
SIN	Sine
COS	Cosine
TAN	Tangent
DTR	Degree → Radian
RTD	Radian → Degree
MCLR	Master Clear, resets all internal registers
ECLR	Error Clear, resets error flag
IN	Synchronous data input instruction
OUT	Synchronous data output instruction
TOGM	Toggle between Scientific and Floating Point Mode
SMDC (DIGIT)	Set Mantissa digit count followed by a digit number
INV	For inverse trigonometry

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NCU BLOCK DIAGRAM AND DESCRIPTION

On the left of *Figure 1*, there are 6 input lines which are used to input instructions and data. These have internal pull-up resistors and can be driven directly from TTL except for I_6 input which requires external 10 kΩ pull-up resistors. POR input may be used to externally reset the chip, and it may be left open when not used. Internal circuit provides automatic initialization at power-up.

The ISEL and R/$\overline{W}$ outputs are not TTL compatible. They source a minimum of 30 μA and sink a minimum of 5 μA. Interfacing to DM74LS series TTL is shown in the interface schematic. ISEL remains high on all 1-word instructions and lowers during the data portion of 2-word instructions. Its usefulness is primarily in stand-alone systems where ISEL line may be used to switch between program store and data store. R/$\overline{W}$ line provides 1 microcycle wide negative pulse during each valid digit period of Out instruction, most applicable in a stand-alone system where this output is used to clock in data.

HOLD input can be driven by TTL. The NCU suspends its data inputting operation when input is set high. The input may be utilized with the RDY output line to input data in handshake mode.

$\overline{DAS}$ output requires a pull-down resistor to drive a DM74LS series component. It sources 500 μA and sinks 5 μA. The line pulses during synchronous data input and output operations. $\overline{BR}$ is a branch condition output which lowers if the state of conditioned branch instruction is true. Its function is primarily in a stand-alone system. It sources 100 μA and typically sinks 15 μA.

An internal 4-phase clock generator drives the NCU. Its input frequency must be provided externally via OSC input, and can be driven with a TTL. Input frequency is typically at 400 kHz. The sync output functions as a synchronizer of external circuits. Its period is 4 clock cycles wide with a negative pulse width of about 1 clock cycle. Output drive characteristics are the same as $\overline{BR}$ output.

The NCU operates with a single supply of 7.9V to 9.5V or a dual supply of 5V and −3.5V ±0.5V. The typical supply current is 12 mA.

F1, F2 and Error outputs are open drain outputs sourcing 6 mA typically. Flag control instructions within NCU control F1 and F2. Error output goes high during improper entry or when computed result exceeds limit. It resets by an error clear (ECLR) or a master clear (MCLR) instruction.

The digit address outputs (DA1–DA4) indicate digit position in BCD during synchronous digit input and output operations. The outputs need not be used in a microprocessor driven system.

Finally, 4 digit output parts (DO1–DO4) send out 4-bit BCD digits during output operation. They are open drain outputs with typical source current of 6 mA.

There are a total of 8 internal registers, each 12 digits deep of which 5 are user accessible. Under program control, data may be swapped and rotated among registers.

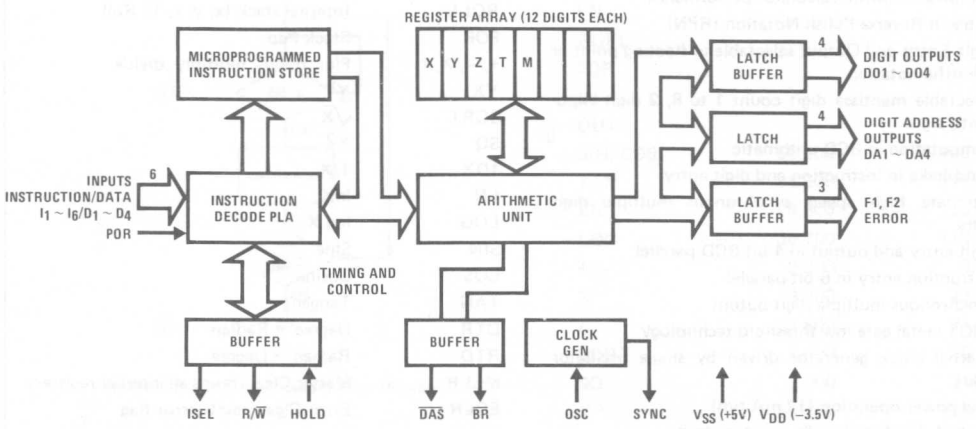

FIGURE 1. Number Cruncher Unit (MM57109) Block Diagram

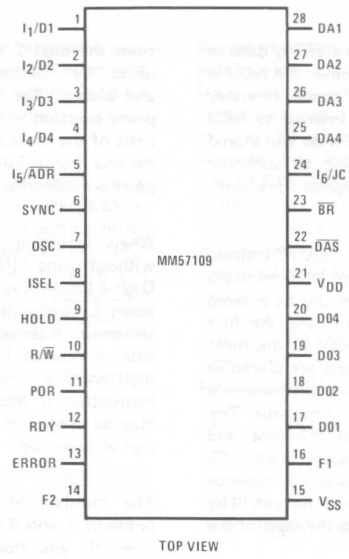

FIGURE 2. NCU Connection Diagram

PINOUT DESCRIPTION

The NCU is housed in a 28-pin dual-in-line plastic package. Each pin name and function is described below.

PIN	NAME	SIMPLIFIED DESCRIPTIONS
1–4	I_1–I_4, D1–D4 Input	Digit input D1=LSB, lower 4 bits of instruction input.
5	I_5, Input	5th bit of instruction input for external synchronization if necessary.
6	Sync Out	400 kHz nominal frequency input.
7	OSC Input	Useful in stand-alone sysem application.
8	ISEL Output	High during instruction input. Low during data input.
9	HOLD Input	(When set high) puts NCU in Wait mode
10	R/W Output	Pulses low to indicate valid digit during "OUT" instruction execution.
11	POR Input	(When set high) NCU is initialized. Same is performed internally at power up.
12	RDY Output	When high indicates that NCU is ready for next input. If hold=low, will input data from the bus. If hold=high, holds in wait mode.
13	ERROR Output	Set high when error condition is detected ECLR instruction must be executed to clear the flag.
14	F2 Output	General purpose flag, under program control. Useful in a stand-alone system application.
15	V_{SS} Input	Most positive supply input V_{SS}–V_{DD} = 8.5V ±0.5
16	F1 Output	General purpose flag output
17–20	DO1–DO4 Output	BCD digit output DO4 = MSB
21	V_{DD} Input	Most negative supply input
22	$\overline{DAS}$ Output	Indicates valid digit address output during "IN" or "OUT" instruction.
23	$\overline{BR}$ Output	Indicates program branch when low. Useful in stand-alone system applications.
24	I_6 Input	MSB of instruction input.
25–28	DA4–DA1 Output	Digit address output during "IN" or "OUT" instruction. Useful in stand-alone system applications.

INPUT OUTPUT DATA FORMAT

There are two basic formats when transferring data to and from the NCU. It depends on whether the NCU is in scientific or floating point notation mode. In either case data transfers between X-register internal to NCU and outside. The X register is 12 digits wide and stored data are different from floating point to scientific notation mode. The data format in X register for scientific notation mode is shown below.

When transferring digits using "IN" or "OUT" instruction, begin with the digit zero. A total of MDC +4 digits are transferred. Data and instructions may also be entered without using "IN" instruction. In this case, the first digit entered is placed in digit 4 location as the most significant mantissa digit. Following digits are placed in successive locations. EE instruction will place following digits in locations zero and one as an exponent. The NCU assumes positive sign for both mantissa and exponent, by placing zeroes in respective places. CS instruction may be used at any part of the entry sequence to change sign of either mantissa or exponent. The decimal point is placed automatically to the right of the most significant mantissa digit.

Input output data format for floating point notation mode is shown below.

In floating point notation digits 0 and 1 are not used. When transferring digits using "IN" or "OUT" instructions the digit 2 is moved first. Before inputting digits using "IN", decimal point position must be computed and placed. The figure above shows that the decimal point position = 11 indicates that the point is to the right of the most significant digit, Digit 4. To move the decimal point further to the right the number in the position indicator must be correspondingly decreased.

When inputting digits in an asynchronous manner without using "IN", the first digit entered is placed in Digit 4 location as the most significant digit. The decimal point (.) instruction may be placed during digit entry sequence. Internally, the decimal point position indicator is reset at 11 and starts counting down with each digit entry and stops counting when the decimal point instruction is inputted. Change sign (CS) instruction may be used to change signs. The NCU assumes positive sign at power-up.

The number of digits transferred is programmable between 1 and 8 using SMDC instruction. On both the scientific and floating point input output operations, internal computation is always carried out in scientific notation mode. At power-up or initialization, the NCU comes up in floating point input output mode. It can be changed by using TOGM (toggle mode) instruction. Also, at power-up the NCU comes up at 8 mantissa digit mode. SMDC instruction may be used to change this.

DIGIT POSITION (IN X REGISTER)	DESCRIPTION AND BIT LOCATION D04 D03 D02 D01
0	Most significant exponent digit (0–9)
1	Least significant exponent digit (0–9)
2	SM 0 0 SE
3	Not used
4	Most significant mantissa digit
.	(Decimal point placed following this digit internally)
.	.
.	.
.	.
MDC + 3	Least significant mantissa digit

Notes: SM = Sign of mantissa 0 = +, 1 = –
SE = Sign of exponent
MDC = Mantissa digit count $1 \leq MDC \leq 8$ MDC is set at 8 at power up

FIGURE 3. Input Output Data Format for Scientific Notation Mode

DIGIT POSITION (IN X REGISTER)	DECIMAL POINT POSITION	DESCRIPTION AND BIT LOCATION D04 D03 D02 D01
2		Sign (0 = plus, 1 = minus)
3		Decimal point position indicator (DPP)
4	11	Most significant mantissa digit
5	10	Next significant mantissa digit
.	.	.
.	.	.
.	.	.
MDC + 3	12-MDC	Least significant mantissa digit

FIGURE 4. Input Output Data Format for Floating Point Notation Mode

INTERFACE LOGIC

Figure 5 shows interface to SC/MP 8-bit microprocessor. The schematic in general, however, is applicable to most microprocessors with 8-bit or more data width. The 8-bit bidirectional data bus of SC/MP handles most communications.

The data going to 6 line data and instruction input, I_1–I_6, are latched by the hex latch device, DM74LS174. When ready to send data out to NCU, the output device must be addressed first. The address decoder, DM7442, is used to decode 4 bits of the address lines. In this case, setting up only the upper bytes of the address register is adequate. Typical instruction sequence for SC/MP might be:

LDI	OUTDATA	:	LOAD ACC with device select address
XPAH	PI	:	store in upper byte of pointer 1
LD	DATA	:	LOAD ACC with data to be sent out
ST	0(P1)	:	SEND data out

During execution of the "ST" instruction, the "out data enable" input lowers. When data on the bus, DB0–DB7, become valid, the "write data strobe" signal pulses low, causing data to latch onto DM74LS174. External 10 kΩ pull-up resistor is required on I_6 input. To load data and status signals from NCU, the octal TRI-STATE buffer, DM81LS95, is used. Output of the buffer is normally disabled. An indexed load instruction with upper index register set-up to input address enables both G1 and G2 inputs of the buffer gating data on to the bus. Typical instruction sequence might be:

LDI	DATAIN	:	load upper pointer with the
XPAH	P1	:	device address
LD	@(P1)	:	load data "IN" from the bus and
ST	@1(P2)	:	store in consecutive locations of memory

To drive the low power Schottky buffer, 10 kΩ pull-down resistors are necessary at the output of NCU.

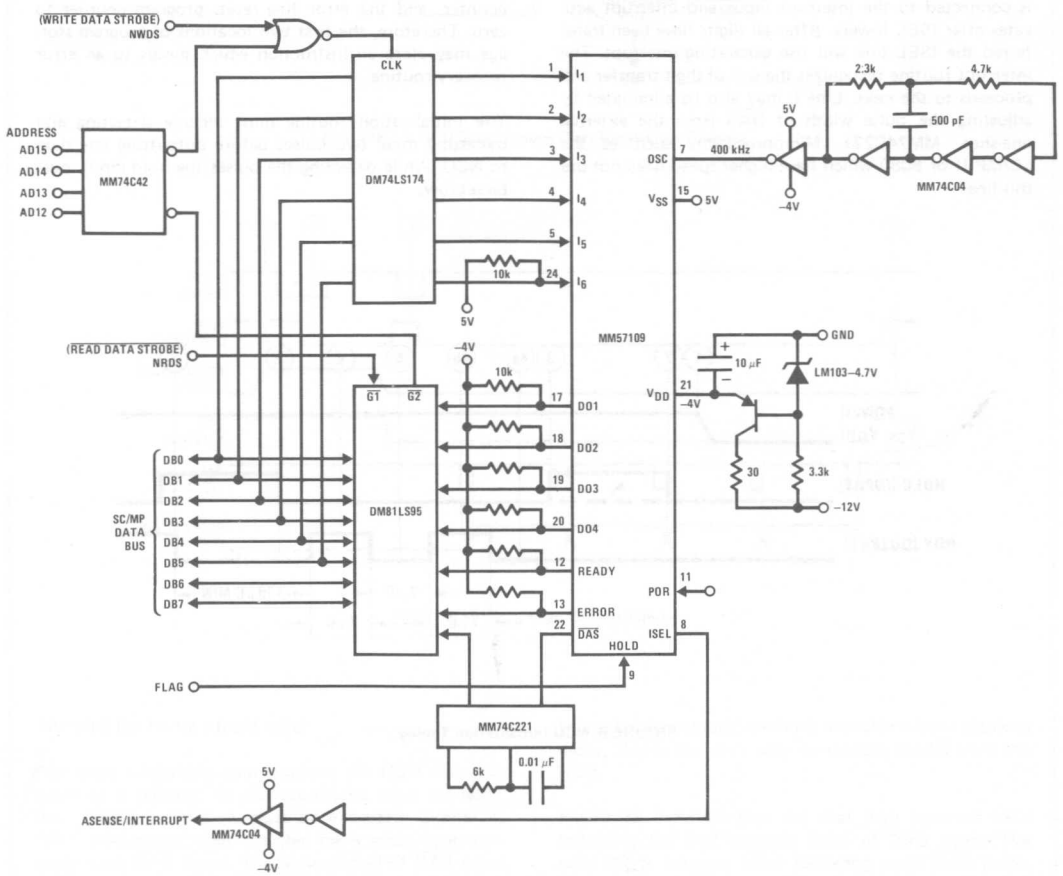

FIGURE 5. NCU Interface to SC/MP

The $\overline{DAS}$ (pin 22) output provides negative-going pulses of 10 μs width between each digit outputted. The 10 μs pulse width is too narrow for most microprocessors to sense. Therefore, "one-shot" is used to stretch the pulse width to 60 μs. The ISEL (pin 8) output drives SENSE 1/interrupt combination input of SC/MP. The NCU spits out new data every 140 μs at an uncontrollable speed. During the 140 μs period the following routine should be performed:

a. Test $\overline{DAS}$ low, loop if not.
b. Test $\overline{DAS}$ high, loop if not.
c. Load data in and increment memory location.
d. Update digit count and check if all digits are in. Exit if done.
e. Jump back to a.

In the case of SC/MP, the above routine cannot be performed in 140 μs. Therefore in the programming, line d was eliminated. To determine the end of digit transfer the ISEL line is tested. At the beginning of digit output sequence the ISEL line lowers. It remains low during transfer period and rises after all digits have been transferred. Refer to timing diagram for data output sequence for this relationship. The ISEL line is connected to the interrupt input and interrupt activates after ISEL lowers. After all digits have been transferred the ISEL line will rise generating interrupt. The interrupt routine recognizes the end of digit transfer and proceeds to the next. Line b may also be eliminated by adjusting the pulse width of $\overline{DAS}$ from the external one-shot, MM74C221. Microprocessors such as the SC/MP II or 8080 which have higher speed need not use this line.

The NCU performs internal initialization when power comes up. Normally, external initialization through POR input is not necessary (pin 11). The input may be left open where not used.

The range of supply voltage at V_{DD} (pin 21) input is $-2.9V \sim -4.5V$. The circuit shows one way of generating $-4V$. The signal at OSC input (pin 7) needs only to swing between 0V V_{SS}. Input, however, is connected to internal pull-up resistor 6 kΩ typical. The CMOS oscillator circuit connected between 5V and $-4V$ ensures meeting the requirement. To slow down NCU, simply lower the oscillator frequency.

NCU INITIALIZATION

The NCU is initialized automatically at power-up. Raising POR (pin 11) input high for a minimum of 8 clock periods will do the same. Status outputs go to zero except $R/\overline{W}$ output which goes to 1. The ready line pulses high twice before it readies to accept data. Refer to timing diagram in *Figure 6*, and flow chart in *Figure 7*.

Two pulses are necessary when the NCU functions in a stand-alone system where RDY line updates a program counter, and the error flag resets program counter to zero. Therefore, the first two locations of program storage may store an instruction which jumps to an error recovery routine.

The initialization routine must include detecting and bypassing these two pulses before outputting any data to NCU. While detecting the pulses the hold input must be set low.

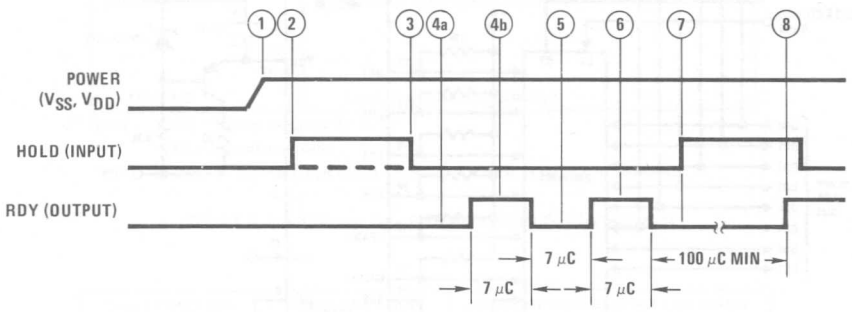

FIGURE 6. NCU Initialization Timing

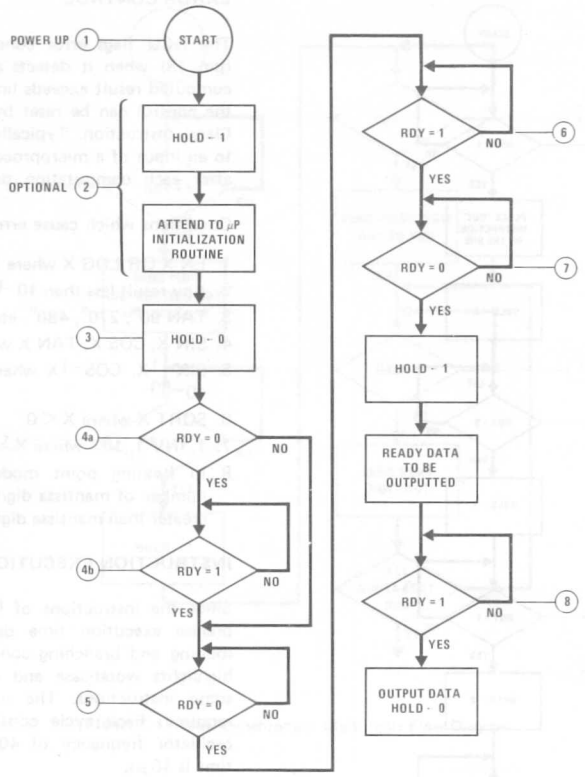

FIGURE 7. NCU Initialization Flow Diagram

SENDING INSTRUCTION AND DATA OUT TO NCU

The timing sequence for outputting digits and all 1-word instructions to NCU is shown in *Figure 8. Figure 9* illustrates the same sequence in flow diagram. One digit or instruction at a time is sent out by handshaking. When the NCU is ready for the next input it raises the RDY line and tests the hold input. If the hold input is high, the NCU waits until it lowers. Then it lowers the ready line and samples the input data. Depending on instructions it may sample input more than once. This necessitates the use of a latch device at the input.

The fastest NCU operation is obtained by maintaining hold input low at all times. This would be an acceptable approach if other routines are not performed during this operation. In this mode the next digit must be ready for output before the RDY line goes up. Each digit entry in this mode takes about 2.4 ms. Other instructions take variable lengths of time.

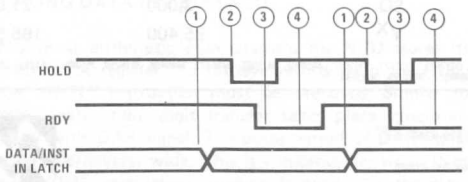

FIGURE 8. NCU Digit and Instruction Input Timing

There are 2 other ways of inputting digits. One of these is also called the "synchronous digit input", requiring the use of input instruction "IN". In this method, the NCU must be informed of exact mantissa digit count through the instruction "SMDC", followed by the digit count. The digits, mantissa, and exponent, if any, and signs must follow a certain format. Refer to input output data format. In this mode, digits are transferred at a fixed rate, and no handshaking is involved. The advantage of this method is the speed of digit input. To enter a signed 8-digit mantissa with signed 2-digit exponent takes about 6 ms. To do the same using the handshaking method will require about 30 ms. The timing sequence and flow diagram performing synchronous digit output are shown in *Figures 10 and 11*, respectively.

In the timing sequence of *Figure 10* the NCU samples digits 1 microcycle after the rising edge of $\overline{\text{DAS}}$ signal. Therefore, the first digit must be ready prior to the rising edge of the first $\overline{\text{DAS}}$ pulse. The pulse width of $\overline{\text{DAS}}$ signal is 1 microcycle wide, and the period of the pulse is 10 microcycles wide. Assuming 10 microseconds for each cycle, the digit period becomes 100 μs. During this period, the system must test $\overline{\text{DAS}}$ = 0, send the next digit out, test that all digits are sent out, then jump back for the next digit if not finished. For slow processing systems this task proves to be very difficult.

At point 6 of *Figure 10*, the NCU is ready for the next instruction.

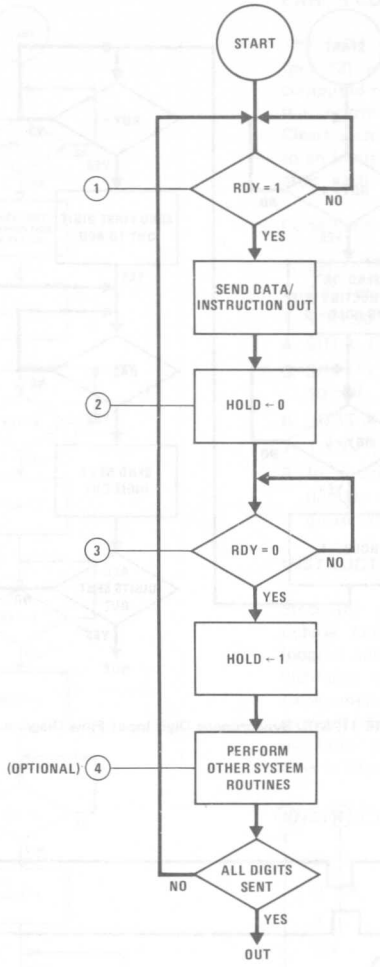

FIGURE 9. NCU Digit and Instruction Input Flow Diagram

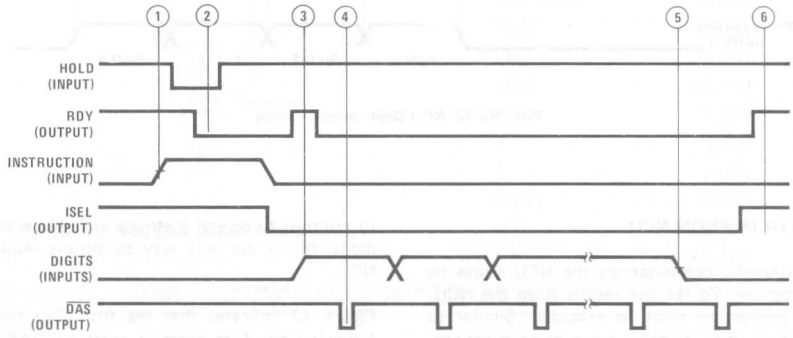

FIGURE 10. NCU Synchronous Digit Input Timing Using "IN" Instruction

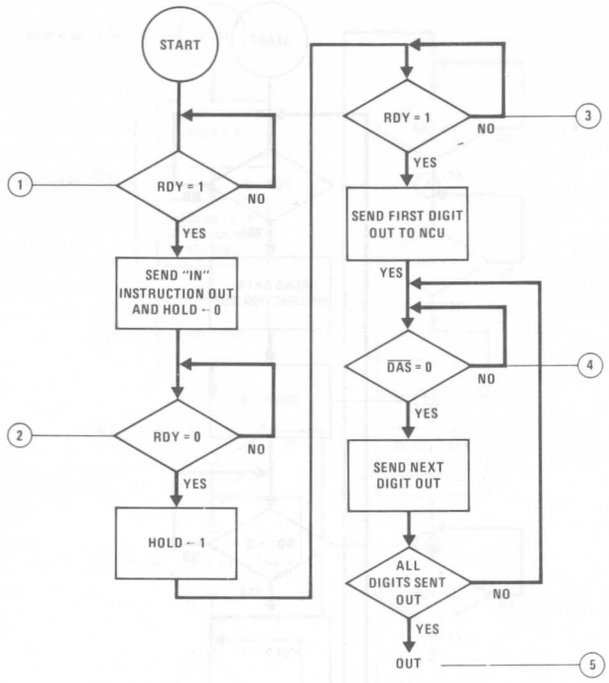

FIGURE 11. NCU Synchronous Digit Input Flow Diagram

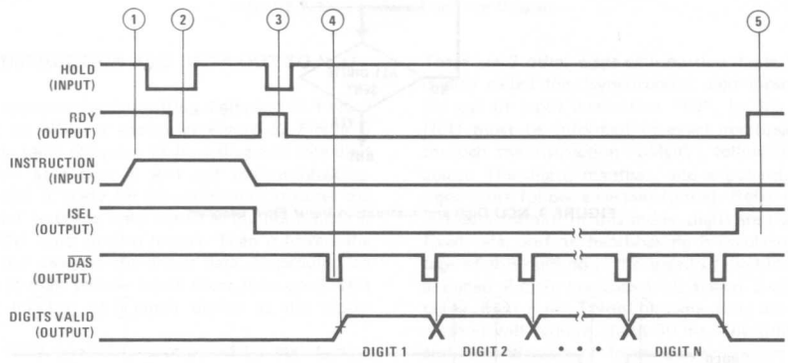

FIGURE 12. NCU Digit Output Timing

TAKING DATA IN FROM NCU

For most arithmetic computations the NCU stores its result in X register. To retrieve results from the NCU, the "OUT" instruction must be executed. Similar to "IN" instruction, digit transfer takes place synchronously with $\overline{\text{DAS}}$ signal. The pulse period of $\overline{\text{DAS}}$ signal is 14 microcycles wide. This is 4 microcycles wider than with "IN" instruction, making it easier for the slow system to respond.

In contrast to several methods available when inputting digits, this is the only way to retrieve results from the NCU.

Figure 12 indicates that the first digit becomes valid following the first negative pulse of $\overline{\text{DAS}}$ signal. The next digits become valid following each $\overline{\text{DAS}}$ pulse. Output signal formats differ between scientific and floating point notations. Further discussion on output signals is found in the input output data format section.

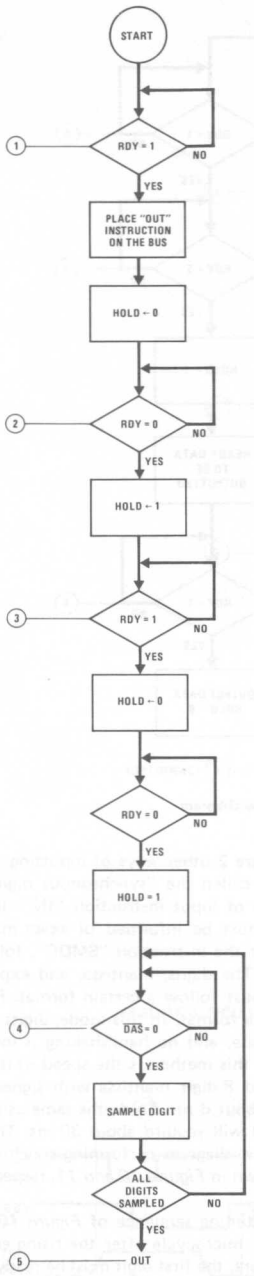

FIGURE 13. NCU Digit Output Flow Diagram

ERROR CONTROL

The NCU flags error condition through error output (pin 13) when it detects a wrong entry, or when the computed result exceeds limit. When an error is flagged the control can be reset by executing an ECLR (Error Clear) instruction. Typically the error flag is connected to an input of a microprocessor. The line may be tested after each computation prior to "OUT" instruction.

Conditions which cause error output (1) are as follows:

1. LN X OR LOG X where $X \leq 0$
2. Any result less than 10^{-99} or greater than 10^{99}
3. TAN 90°, 270°, 480°, etc.
4. SIN X, COS X, TAN X where $|X| \geq 9000$
5. $SIN^{-1}X$, $COS^{-1}X$ where $X < -1$ or $X > 1$ or $X \leq 10^{-50}$
6. SQRT X where $X < 0$
7. 1, INV 1, 10X where X = 0
8. In floating point mode, OUT instruction if the number of mantissa digits to left of decimal point is greater than mantissa digit count.

INSTRUCTION EXECUTION TIME

Since the instructions of NCU are microprogrammed, precise execution time depends on various internal looping and branching conditions. The following table highlights worst-case and average execution times of some instructions. The unit is in execution cycles required. Each cycle consists of 4 clock periods. At oscillator frequency of 400 kHz the execution cycle time is 10 μs.

INSTRUCTION	EXECUTION TIME (IN MICROCYCLES)	
	Average	Worst-Case
0 ~ 9		238
π		1,312
EN		552
ROLL		905
POP		448
IN		395
OUT		583
SIN, COS	56,200	195,900
TAN	35,000	117,600
LN	24,800	115,000
LOG	30,700	113,500
+, −	2,200	6,600
X	3,200	22,700
/	7,800	21,400
SQRT	7,000	30,200
SQ	3,000	21,900
Y^X	55,400	195,500

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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