CUSTOM ROM PROGRAMMING

INTRODUCTION

Custom ROM programs are submitted to National in three formats: paper tape, punched cards or truth table with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable gate mask and the test tape. Wafers are held in inventory at gate mask. The wafers are then completed using the custom gate mask and tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly the units are tested using the custom test tape to assure the correct output pattern for every address.

When MOS was in its infancy the design engineers called a logic ONE a low voltage because a P-channel MOS transistor is turned on with a negative bias applied. This became known as NEGATIVE logic and was the opposite of TTL's POSITIVE logic. As the MOS technology evolved and TTL compatibility became a reality it became desirous to use the same logic in MOS as in TTL. Therefore the first ROMs to come out were specified in NEGATIVE logic and the new ROMs are specified in POSITIVE logic. Extra care must be taken in entering ROM codes that it is clear which logic level is used. National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic but the customer must specify which logic it is.

DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input Output Definitions

Address: A_1 is the least significant input address on ROMs. L_0 is the least significant input address on character generators.

Outputs: B_1 is the least significant output.

INFORMATION NEEDED

So that National can better serve its customers the following information *must* be submitted with each ROM code.

National Semiconductor Corporation
2900 Semiconductor Dr., Santa Clara, CA 95051
Phone (408) 732-500 TWX 910-339-9240

				NATIONAL PART NUMBER
				ROM LETTER CODE (NATIONAL USE ONLY)
NAME				DATE
ADDRESS				CUSTOMER PRINT OR I.D. NO.
CITY		STATE	ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE		DATE

TRUTH TABLE FORMS

Use the appropriate form for submitting truth tables.

Form I

MM3501	MM5204	MM4214/MM5214	MM4231/MM5231
MM5201	MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM5202	MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4203/MM5203	MM4213/MM5213	MM4230/MM5230	

ADD-RESS	OUTPUT CODE NOTE: 1 B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __0									
__ __1									
__ __2									
__ __3									
__ __4									
__ __5									
__ __6									
__ __7									
__ __8									
__ __9									
__ 10									
__ 11									
__ 12									
__ 13									
__ 14									
__ 15									
__ 16									
__ 17									
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__ 42									
__ 43									
__ 44									
__ 45									
__ 46									
__ 47									
__ 48									
__ 49									
TB									

ADD-RESS	OUTPUT CODE B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50									
__ 51									
__ 52									
__ 53									
__ 54									
__ 55									
__ 56									
__ 57									
__ 58									
__ 59									
__ 60									
__ 61									
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__ 84									
__ 85									
__ 86									
__ 87									
__ 88									
__ 89									
__ 90									
__ 91									
__ 92									
__ 93									
__ 94									
__ 95									
__ 96									
__ 97									
__ 98									
__ 99									
TB									

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Addresses and Outputs
- ☐ NEGATIVE Logic on Addresses and Outputs

Note 2: The MM4232/MM5232 and MM4233/MM5233 have programmable chip selects and the logic level to enable the chip must be specified. CS 1 __ CS 2 __ CS 3 __ CS 4__

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form II

MM5212
MM5215
MM4229/MM5229 (Positive logic only)

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ __ 0													
__ __ 1													
__ __ 2													
__ __ 3													
__ __ 4													
__ __ 5													
__ __ 6													
__ __ 7													
__ __ 8													
__ __ 9													
__ 10													
__ 11													
__ 12													
__ 13													
__ 14													
__ 15													
__ 16													
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__ 38													
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__ 41													
__ 42													
__ 43													
__ 44													
__ 45													
__ 46													
__ 47													
__ 48													
__ 49													
TB													

ADDRESS	OUTPUT CODE NOTE: 1 B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	LSB B1	SUM
__ 50													
__ 51													
__ 52													
__ 53													
__ 54													
__ 55													
__ 56													
__ 57													
__ 58													
__ 59													
__ 60													
__ 61													
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__ 87													
__ 88													
__ 89													
__ 90													
__ 91													
__ 92													
__ 93													
__ 94													
__ 95													
__ 96													
__ 97													
__ 98													
__ 99													
TB													

Note 1: The Appropriate Logic Level box must be checked or order will *not* be accepted.
- ☐ POSITIVE Logic on Address and Outputs
- ☐ NEGATIVE Logic on Address and Outputs

Note 2: The MM4229/MM5229 has programmable chip selects. Specify the Logic Level to enable the Chip (Positive Logic)
CS 1 ___ CS 2 ___ CS 3 ___

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form III

MM4240/MM5240

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_0	0 ($L_2L_1L_0$ 000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_1	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_2	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
_3	0 (000)						
	1 (001)						
	2 (010)						
	3 (011)						
	4 (100)						
	5 (110)						
	6 (110)						
	7 (111)						
	TB						

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_4	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_5	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_6	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_7	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	TB						

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS (DECIMAL)	OUTPUT WORD B_1	B_2	B_3	B_4	B_5	SUM
_8	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
_9	0						
	1						
	2						
	3						
	4						
	5						
	6						
	7						
	TB						

Note 1: A logic "1" = most negative voltage. A logic "0" = most positive voltage.

Note 2: Line address (L_0, L_1, L_2) are the row or column select lines in a character generator application. In a read only memory application, A_5 shall be considered the MSB and L_0 the LSB.

Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

Form IV

MM4241/MM5241

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_0	0 (L_2 L_1 L_0 0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_1	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_2	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 1 0)									
_3	0 (0 0 0)									
	1 (0 0 1)									
	2 (0 1 0)									
	3 (0 1 1)									
	4 (1 0 0)									
	5 (1 0 1)									
_4	0									
	1									
	2									
	3									
	4									
	5									
	TB									

CHARACTER ADDRESS (DECIMAL)	LINE ADDRESS DECIMAL	LSB B1	B2	B3	B4	B5	B6	B7	B8	SUM
_5	0									
	1									
	2									
	3									
	4									
	5									
_6	0									
	1									
	2									
	3									
	4									
	5									
_7	0									
	1									
	2									
	3									
	4									
	5									
_8	0									
	1									
	2									
	3									
	4									
	5									
_9	0									
	1									
	2									
	3									
	4									
	5									
	TB									

Note 1: On the character address and output word negative logic is used:
A logic "1" most negative voltage
A logic "0" most positive voltage
on the line address positive logic is used:
A logic "0" most negative voltage
A logic "1" most positive voltage

Note 2: Line address (L_0, L_1, L_2) are the column select lines in a character generator application. In a read only memory application A_6 shall be considered the MSB and L_0 the LSB.

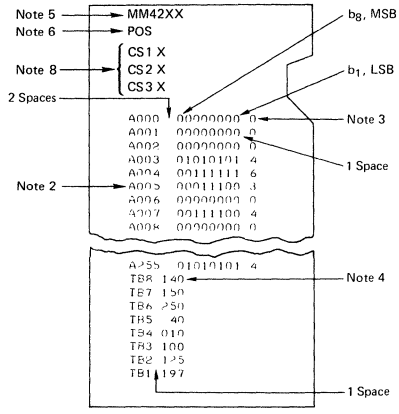
Note 3: TB is the total "1" bits in a column expressed in Decimal.

Note 4: SUM is the total "1" bits in a row expressed in Decimal.

TAPE ENTRY FORMAT

Tape format for the following ROMs.

MM3501	MM4214/MM5214	MM4231/MM5231
MM4210/MM5210	MM4220/MM5220	MM4232/MM5232
MM4211/MM5211	MM4221/MM5221	MM4233/MM5233
MM4213/MM5213	MM4230/MM5230	



8-BIT TAPE FORMAT

Note 1: The code is a 7-bit ASCII code on 8 punch tape.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number if "1" bits in each output column or bit position.

Note 5: Specify product type.

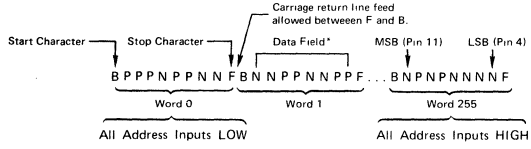
Note 6: Must type POS logic, or NEG logic depending on which is used.

Note 7: LOGIC ON ADDRESS AND OUTPUTS must be the same (either POS or NEG).

Note 8: Specify the pattern necessary to enable the ROM on the ROMS that need chip selects.

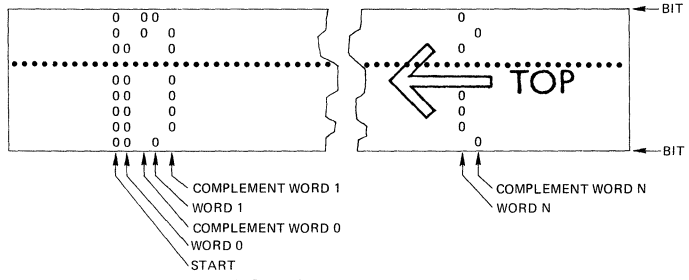
Tape format for the MM5202, MM4203/MM5203 and MM4204/MM5204.

PROM TAPE P AND N FORMAT



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start be rubbed out. Data for exactly 256 words must be entered, beginning with word 0. P = "1" or the more positive voltage. N = "0" or most negative voltage. When the MM4204/MM5204 is used the word length is 512.

PROM TAPE BINARY FORMAT



Note 1: Tape must be all blank except for the 513 words punched.

Note 2: Tape must start with a START punch.

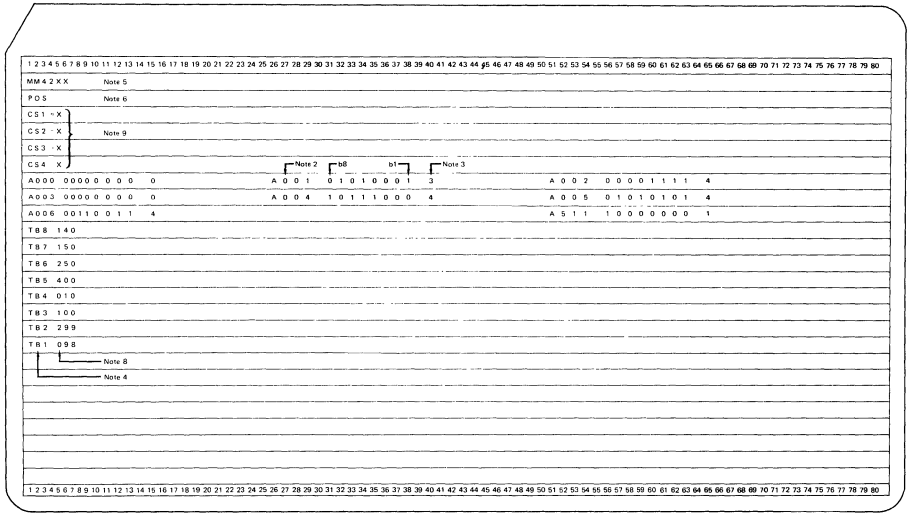
Note 3: Data is comprised of two words the first being the actual Data the second being the complement of the data.

Note 4: A punch is equal to a "1" or most positive voltage and the omission of a punch is a "0" or the more negative voltage.

When programming the MM5202 or MM4203/MM5203 it should be remembered that the opposite logic from what is programmed will appear on the output of the PROM. In otherwords a P on the tape will program a Logic "0" or V_L in the PROM.

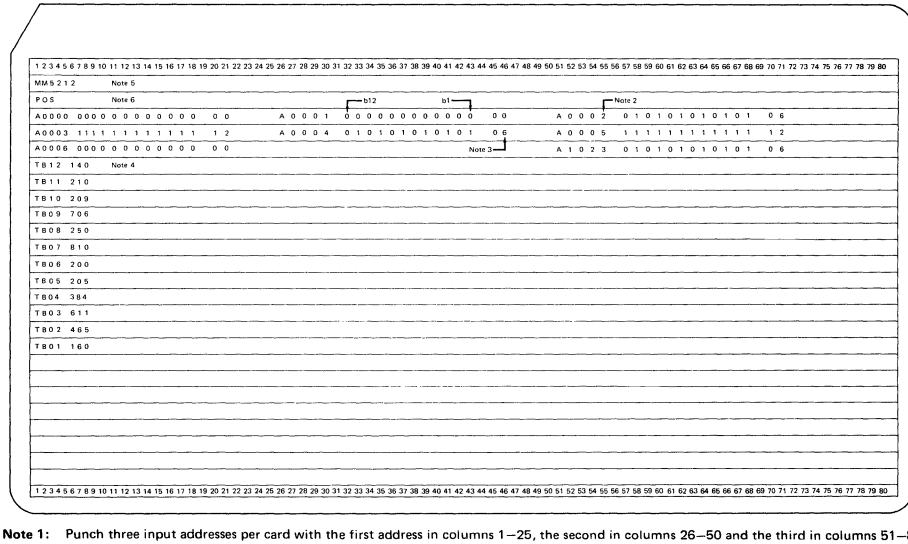
CARD ENTRY FORMAT

Card format for the: MM3501, MM4210/MM5210, MM4211/MM5211, MM4213/MM5213, MM4214/MM5214, MM4220/MM5220, MM4221/MM5221, MM4230/MM5230, MM4231/MM5231, MM4232/MM5232, MM4233/MM5233



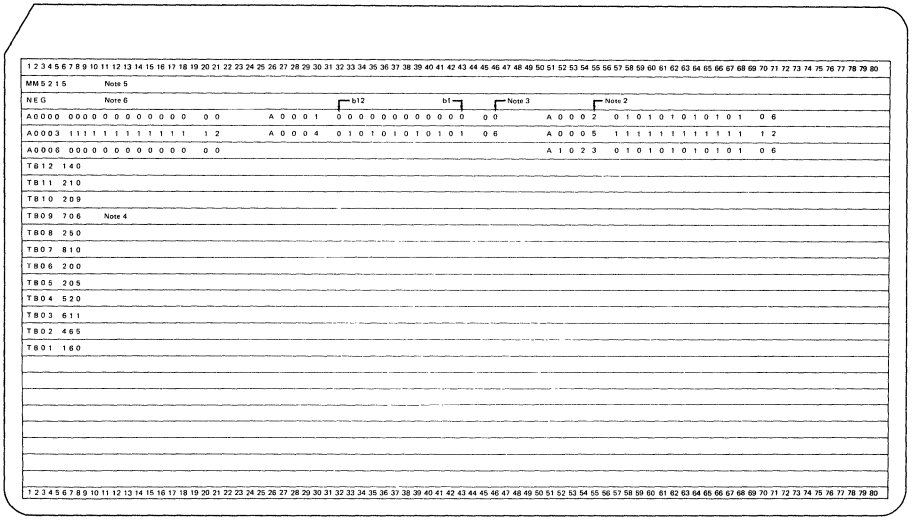
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic or NEG logic depending on which is used.
Note 7: LOGIC ON ADDRESS, OUTPUTS AND CHIP ENABLE must be the same (either POS or NEG).
Note 8: Leading zeros must be punched.
Note 9: Specify the Chip Select Logic Levels that will enable the ROM where necessary.

Card format for the MM5212.



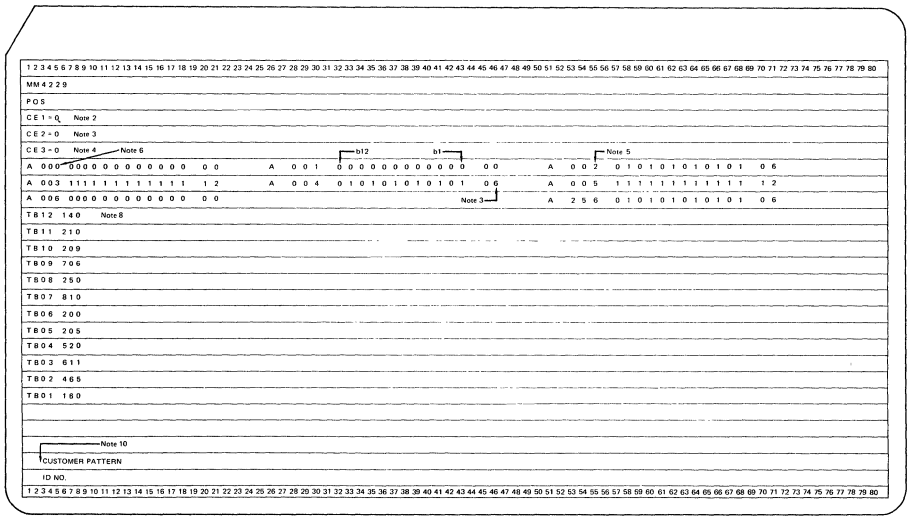
Note 1: Punch three input addresses per card with the first address in columns 1–25, the second in columns 26–50 and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type POS logic.
Note 7: POSITIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more positive output. "0" more negative output.
Note 9: Leading zeroes must be punched.

Card format for the MM5215.



Note 1: Punch three input addresses per card with the first in columns 1–25, the second in columns 26–50, and the third in columns 51–80.
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 3: The total number of "1" bits in the output word.
Note 4: The total number if "1" bits in each output column or bit position.
Note 5: Specify product type.
Note 6: Must type negative logic.
Note 7: NEGATIVE LOGIC ON ADDRESS AND OUTPUTS.
Note 8: "1" more negative output, "0" more positive output.
Note 9: Leading zeroes must be punched.

Card format for the MM4229/MM5229.



Note 1: The code is Hollerith as punched on IBM Model 029.
Note 2: Corresponds to Pin 16
Note 3: Corresponds to Pin 15
Note 4: Corresponds to Pin 14
Note 5: The ROM input address is expressed in decimal form and is preceded by the letter A.
Note 6: All 256 address (0–255) must be coded.
Note 7: The total number of "1's" in each input word.
Note 8: The total number of "1's" in each output column.
Note 9: Leading zeros must be punched.
Note 10: The customer may use his own ID designation if he does not punch the first column.
Note 11: Positive logic on address and outputs "1" more positive voltage "0" more negative voltage.